Performance of Multiple-Bus Multiprocessor Under Non-Uniform Memory Reference Model

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ABSTRACT

Performance evaluation of multiple-bus multiprocessor systems is usually carried out under the assumption of uniform memory reference model. Hot spots arising in multiprocessor systems due to the use of shared variables, synchronization primitives etc., give rise to non-uniform memory reference patterns. The objective of this paper is to study the performance of multiple bus multiprocessor system in the presence of hot spots. Analytic expressions for the average memory bandwidth and probability of acceptance of prioritized processors have been derived. The results are validated by simulation results.
Keywords: Multiple bus interconnection, performance evaluation, memory bandwidth, blocking probability, multiprocessors.