Modified cut-set matrix of an n-port network

P. Thulasiraman, B.E., M.Sc.(Eng.), and V. G. K. Murti, B.E., M.Eng., Ph.D.

Synopsis

The modified cut-set matrix of an n-port network is defined and its properties are enumerated. The importance of this concept in considering the parallel interconnection of n-port networks containing R, L and C elements is demonstrated. A procedure is obtained for the generation of a class of continuously equivalent networks of a given RLC n-port network. The class is characterised by the property that all networks belonging to this class have the same modified cut-set matrix. Using this procedure, it can be shown that, for a resistive n-port network in which every pair of vertexes is connected by a finite positive conductance, a large number of continuously equivalent networks containing only nonnegative conductances can always be obtained. The usefulness of this result in the synthesis of RLC n-port networks is indicated.

List of symbols

n = number of ports
e = number of edges in the graph of the network
v = number of vertexes
v_1 = number of external vertexes
v_2 = number of internal vertexes
V_e = column matrix of Laplace transforms of edge voltages
V_t = column matrix of Laplace transforms of voltages of branches of a tree; submatrix of V_e
V_p = column matrix of Laplace transforms of port voltages; submatrix of V_t
V_n = column matrix of Laplace transforms of nonport branch voltages; submatrix of V_t
I_e = column matrix of Laplace transforms of edge currents
I_s = column matrix of Laplace transforms of currents in the sources across the branches of a tree
I_p = column matrix of Laplace transforms of port currents; a submatrix of I_s
C_0 = fundamental cut-set matrix
C_1 = submatrix of C_0 comprising the rows corresponding to port branches
C_2 = submatrix of C_0 comprising the rows corresponding to nonport branches
C = modified cut-set matrix
c_{ij} = entry in the ith row and jth column of C
C^1, C^2 = submatrices of C
Y_e = diagonal edge admittance matrix
y_e = column matrix of edge admittances
Y_c = cut-set admittance matrix
Y_{11}, Y_{12}, Y_{21}, Y_{22} = submatrices of Y_c
Y = short-circuit admittance matrix
K = potential-factor matrix with the potential factor K_{ij} as entry in ith row and jth column

1 Introduction

In network studies, an important role is played by the cut-set matrix[1] which represents the constraints imposed on the current variables by the topology of the network. If a set of $v - 1$ sources be connected across the branches of a chosen tree, and C_0 is the fundamental cut-set matrix with respect to this tree, C_0 has the following important properties:

(a) It relates the edge voltages V_e to the branch voltages V_t by

$$V_e = C_0' V_t \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (1)$$

(b) It relates the currents I_s in the sources across the branches to the edge currents I_e by

$$I_s = C_0 I_e \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (2)$$

(c) It relates the cut-set admittance matrix Y_c of the network to the edge-admittance matrix Y_e by the congruent transformation

$$Y_c = C_0 Y_e C_0' \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (3)$$

In the analysis of n-port networks connected to n independent voltage sources, the relationship between the edge voltages and the port voltages, the edge currents and the port currents, and between the port voltages and the port currents, as expressed by the short-circuit admittance matrix Y, are important. If the number of ports n is equal to $v - 1$, the n ports can be taken to form a tree, and the port voltages V_p and the port currents I_p can be identified with V_t and I_t in eqns. 1 and 2, while the short-circuit admittance matrix Y is identified with Y_c in eqn. 3. No matrix inversion is then necessary to evaluate V_e, I_e and I_p. If the number of ports n is less than $v - 1$, the sources across $v - n - 1$ branches of the tree may be assumed to have zero current, but the evaluation of V_e, I_e, I_p and Y is not so simple or direct as before.

Now, in this latter situation, i.e. $n < v - 1$, it is desirable to have another matrix which plays essentially the same role as C_0 does for the case when $n = v - 1$ in relating the edge voltages to the port voltages, the port currents to the edge currents and the port currents to the port voltages by eqns. 1, 2 and 3. Cederbaum[2], in a recent paper on the equivalence of resistive n-port networks, has defined such a matrix and termed it the modified cut-set matrix C. If C, V_p and I_p are used in place of C_0, V_t and I_s, respectively, the formal relations between the port and edge voltages, the port currents and the edge currents and the port currents and voltages fit exactly into the pattern of eqns. 1, 2 and 3. It may, however, be observed that the modified cut-set matrix is not a topological matrix like C_0, in that it depends on the edge admittances, and not solely on the topology, of the network. At the same time, as shown by the authors,[3,4] C assumes a canonical form independent of the actual admittance values for certain classes of networks.

In this paper, certain properties of the modified cut-set matrix C are stated and proved. Two important applications of the modified cut-set matrix are highlighted. One is related to the parallel connection of n-port networks. The preliminary results on this topic already reported by the authors[5] are now generalised and given in a more complete form. The second application is to the generation of equivalent n-port networks, in the context of which the modified cut-set matrix was originally discussed.[2] This work extends the proposals of Cederbaum and the results reported in Reference 3. The class of equivalent networks generated by this method is characterised by the property that all the networks belonging to this class have the same modified cut-set matrix. Using this method, it can be shown that, for a resistive n-port network in which every pair of vertexes is connected by a finite

Paper 5587 E, first received 1st November 1967 and in revised form 9th April 1968
Mr. Thulasiraman and Dr. Murti are with the Department of Electrical Engineering, Indian Institute of Technology, Madras 36, India

positive resistance, a large number of equivalent networks containing only positive resistances can always be obtained. The usefulness of this result will be clear from the following.

The analysis and synthesis of n-port electrical networks is important in such studies as the analogue representation of multiterminal systems and the synthesis of active-filter networks with the active elements terminating certain ports of an RLC multiport network. The realisation of a resistive n-port network is looked on as representing the first step in the synthesis of RLC n-port networks, since such an RLC network displays, for positive real values of the complex frequency variable s, the properties of a resistive network. The properties of resistive n-port networks with more than $n+1$ nodes remains unsolved, although several methods are available to synthetise resistive n-port networks with $n+1$ nodes. The approach suggested independently by Cederbaum[2] and Guillemin[6] to realise a real symmetric matrix Y as the short-circuit conductance matrix of a resistive n-port network with more than $n+1$ nodes consists of two steps. The first step requires the determination of a resistive n-port N_1 having Y as its short-circuit conductance matrix. N_1 may have some negative conductances. The second requires the determination of a resitive n-port network N_2 having a zero conductance matrix, so that the parallel combination of N_1 and N_2 contains only nonnegative conductances. The equivalent-network generation procedure given in this paper offers a solution to the second aspect of this problem.

The symbols I_p, V_p etc. used for currents and voltages are Laplace transforms of the variables. Accordingly, when a voltage source is said to have unit value, the Laplace transform of its voltage is 1. For the case of resistive networks, however, the symbols I_p, V_p etc. may also be interpreted as the actual currents and voltages.

2 Definition and properties of the modified cut-set matrix

Consider an RLC n-port network with v vertexes. We assume that the graph of the network is complete and that the accessible ports of the network can be embedded in a tree of this graph. Edges with zero admittance are permitted, to provide for the general case where the actual network graph is not complete.

If V_e represents the column matrix of edge voltages and V_p represents the column matrix of port voltages, we define the modified cut-set matrix C of an n-port network as the $n \times e$ order matrix, whose transpose C' transforms the matrix V_p into the corresponding matrix V_e by the relationship

$$V_e = C'V_p \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (4)$$

When an n-port RLC network is connected to n specific external voltage sources, except in degenerate cases, the voltage across every edge is uniquely determined and is linearly related to the voltage of each source. Excluding from consideration the special cases, C' is determined uniquely for a given network if its port configuration and the orientations of the ports and edges are specified. If $n = v - 1$, the ports constitute all the branches of a tree, and the edge voltages are uniquely determined by the topological constraints. For a general case, where $n < v - 1$, the port voltages do not by themselves specify all the edge voltages, and hence C depends both on the topology of the network and on the edge admittance values represented by the diagonal matrix Y_e. Following Cederbaum,[2] we next proceed to obtain an expression for C which illustrates this dependence.

Let

$$C_0 = \begin{bmatrix} C_1 \\ \hline C_2 \end{bmatrix}$$

be the fundamental cut-set matrix of the n-port network with respect to a tree which includes the edges shunting the ports. Let the rows of the submatrix C_1 correspond to these edges and those of the submatrix C_2 correspond to the remaining $v - n - 1$ branches of the tree. Let the branches shunting the ports be referred to as the port branches and the rest be referred to as nonport branches. If I_p is the column matrix of port currents and V_n is the column matrix of nonport-branch voltages, we have

$$\begin{bmatrix} I_p \\ \hline 0 \end{bmatrix} = C_0 Y_e C_0' \begin{bmatrix} V_p \\ \hline V_n \end{bmatrix} \quad . \quad . \quad . \quad (5)$$

$$= \begin{bmatrix} C_1 Y_e C_1' & C_1 Y_e C_2' \\ \hline C_2 Y_e C_1' & C_2 Y_e C_2' \end{bmatrix} \begin{bmatrix} V_p \\ \hline V_n \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ \hline Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_p \\ \hline V_n \end{bmatrix}$$

The second set of equations in eqn. 5 yields

$$V_n = -Y_{22}^{-1} Y_{21} V_p \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (6)$$

From eqn. 6 and the following relationship:

$$V_e = C_0' \begin{bmatrix} V_p \\ \hline V_n \end{bmatrix} \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (7)$$

we obtain

$$\begin{aligned} V_e &= C_1' V_p + C_2' V_n = [C_1' - C_2' Y_{22}^{-1} Y_{21}] V_p \\ &= [C_1 - Y_{12} Y_{22}^{-1} C_2]' V_p \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (8) \end{aligned}$$

Comparing eqns. 4 and 8, and recognising that the modified cut-set matrix of a given network is unique, we have the following expression for C:

$$C = C_1 - Y_{12} Y_{22}^{-1} C_2 \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (9)$$

The inverse of Y_{22} exists, except in the singular cases where the nonport branch voltages become indeterminate. In the following, we assume that the inverse of Y_{22} exists.

We next express the short-circuit admittance matrix Y of the n-port network in terms of C and Y_e. From eqn. 6 and the first set of equations in eqn. 5, we obtain

$$\begin{aligned} I_p &= Y_{11} V_p + Y_{12} V_n = [Y_{11} - Y_{12} Y_{22}^{-1} Y_{21}] V_p \\ &= [C_1 - Y_{12} Y_{22}^{-1} C_2] Y_e [C_1 - Y_{12} Y_{22}^{-1} C_2]' V_p \\ &= C Y_e C' V_p \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (10) \end{aligned}$$

In this expression, CY_eC' can be recognised as the short-circuit admittance matrix Y of the n-port network.

We also have the following result:

$$I_p = C Y_e C' V_p = C Y_e V_e = C I_e \quad . \quad . \quad . \quad . \quad . \quad . \quad (11)$$

where I_e is the column matrix of edge currents.

Eqns. 4, 10 and 11 represent the three fundamentally important properties of the modified cut-set matrix, while eqn. 9 may be used for its determination. We now state the property implied by eqn. 4 in the form of a theorem, as it is important in the discussions to follow.

Theorem 1. The element c_{ij} of the matrix C is equal to the voltage appearing across the edge corresponding to column j when port i is excited with a source of unit voltage and all the other ports are short-circuited.

Theorem 2. For the special case of the n-port network with nonnegative resistances, the magnitude of every entry in its modified cut-set matrix is less than or equal to 1.

Proof. The entry c_{ij} represents the voltage across the edge j when port i is connected to a unit-voltage source and all the other ports are short-circuited (theorem 1). Since a resistive network with positive resistances has the well known no-amplification property, the magnitude of any edge voltage in the above cannot exceed 1. Hence the theorem.

Theorem 3. If $M = [m_{ij}]$ be a matrix of order $n \times (v - n - 1)$, such that

(*a*) m_{ij} is equal to the voltage appearing across the jth nonport branch when port i is excited with a source of unit voltage and all the other ports short-circuited

(*b*) the column ordering of M corresponds to the row ordering of C_2 then

$$Y_{12} Y_{22}^{-1} = -M$$

Proof. Let M_i be the ith row of matrix M. Now consider port i to be excited with a source of unit voltage and all the

other ports to be short-circuited. We have $V_n = M'_i$, and also, from eqn. 6, we have

$$M'_i = V_n = -Y_{22}^{-1}Y_{21}V_p = -Y_{22}^{-1}Y_{21}\begin{bmatrix}0\\0\\\cdot\\\cdot\\0\\1\\0\\0\\\cdot\\\cdot\\0\end{bmatrix} \leftarrow i\text{th row}$$

$$= -(i\text{th column of } Y_{22}^{-1}Y_{21})$$

or

$$M_i = -(i\text{th row of } Y_{12}Y_{22}^{-1})$$

Similarly for the other rows of M, and hence the theorem.

Theorem 4. If Y_e is the edge-admittance matrix of a given n-port network, and C its modified cut-set matrix,

$$(a)\ CY_eC'_2 = 0 \text{ and } (b)\ CY_eC'_1 = Y$$

Proof. We have

$$CY_eC'_2 = (C_1 - Y_{12}Y_{22}^{-1}C_2)Y_eC'_2$$
$$= C_1Y_eC'_2 - Y_{12}Y_{22}^{-1}C_2Y_eC'_2 = Y_{12} - Y_{12}Y_{22}^{-1}Y_{22} = 0 \quad \ldots\ (12)$$

Furthermore,

$$Y = CY_eC'$$
$$= CY_eC'_1 - CY_eC'_2Y_{22}^{-1}Y_{21}$$
$$= CY_eC'_1$$

since $C_2Y_eC'_2 = 0$ from eqn. 12 $\quad \ldots\ (13)$

Theorem 5. Given the modified cut-set matrix of an n-port network having specified edge and port orientations, the matrix $Y_{12}Y_{22}^{-1}$ is uniquely determined.

The proof of the theorem follows from theorems 1 and 3.

Theorem 6. Let C be the modified cut-set matrix of a given n-port network N_1. If any diagonal matrix Y_{e2} satisfies the equation $CY_{e2}C'_2 = 0$, the modified cut-set matrix of an n-port network N_2 with Y_{e2} as its edge admittance matrix and having the same port configuration and edge orientation as N_1 is also equal to C.

Proof. From theorem 5, it follows that the matrix $Y_{12}Y_{22}^{-1} = -M$ of the network N_1 is uniquely determined. Its modified cut-set matrix is then equal to $C_1 + MC_2$. Since N_2 has the same port configuration and edge orientation as N_1, the topological matrices C_1 and C_2 are the same for both networks. We now have, for N_2,

$$CY_{e2}C'_2 = (C_1 + MC_2)Y_{e2}C'_2$$
$$= C_1Y_{e2}C'_2 + MC_2Y_{e2}C'_2$$
$$= 0$$

We then obtain

$$(C_1Y_{e2}C'_2)(C_2Y_{e2}C'_2)^{-1} = -M$$

The matrix on the left-hand side of the above equation is recognised as the $Y_{12}Y_{22}^{-1}$ matrix of network N_2. Hence its modified cut-set matrix is $C_1 + MC_2$ and is equal to that of N_1.

Theorem 6 is useful in the generation of equivalent n-port networks to be discussed later.

Definition 1. The potential factor K_{ij} in an n-port network is defined as the potential of the positive reference terminal of port j with respect to the negative reference terminal of port i, when port i is excited with a unit source and all the other ports are short-circuited.

It follows from the definition that K_{ii} is unity. In general, K_{ij} is a function of the complex variable s, but, for a resistive network, K_{ij} is a real number.

Definition 2. An internal vertex of an n-port network is a vertex which is not the terminal of any port.

Definition 3. A vertex of an n-port network which is not an internal vertex is an external vertex.

Let the number of external and internal vertexes in an n-port network be v_1 and v_2, respectively. Obviously, $n + 1 \leqslant v_1 \leqslant 2n$. We partition the matrix C as $[C^1|C^2]$, so that the columns of C^1 correspond to all the edges which are not incident at an internal vertex and the columns of C^2 correspond to the rest. Thus an edge joining an internal and an external vertex belongs to the second group.

In the analysis of n-port networks, it is possible to eliminate the internal vertexes by a generalised star–mesh conversion and consider an equivalent n-port network without internal vertexes. Similarly, in synthesis, if a physically realisable resistive network with internal vertexes exists, another similar realisation without internal vertexes is also possible. Therefore it is permissible to omit any consideration of internal vertexes in n-port-resistive-network studies. However, in the following, the presence of internal vertexes is permitted in the interests of generality. With this approach, the results obtained may be applied directly to any n-port network, without first having to eliminate the internal vertexes. For the particular case of networks without internal vertexes the modified cut-set matrix C itself takes the place of the submatrix C^1 in the theorems that follow.

Theorem 7. Each element of the submatrix C^1 of the modified cut-set matrix C of an n-port network is a linear combination of, at the most, two potential factors K_{ij}. Furthermore, for every $K_{ij}(j \neq i)$ there exist at least two elements of C^1 equal to $\pm K_{ij}$.

Proof. Consider the complete graph formed by all the external vertexes. This is a subgraph of the network graph, and the columns of C^1 correspond to the edges of this subgraph and the n ports of the network can be embedded in a tree of this subgraph. If port i is excited with a source of unit voltage, and all the other ports are short-circuited, it is clear that the voltage across every edge of this graph which is not short-circuited and which is not connected to the negative terminal of port i can be expressed as the difference of two potential factors. An edge incident at the negative terminal of port i joins this terminal to the terminal of some port j. If $j = i$, the voltage across it is equal to K_{ii}, i.e. 1. If $j \neq i$, this voltage is equal to $\pm K_{ij}$, depending on the edge orientation. Since we have assumed a complete graph, there exist two edges joining the negative terminal of port i to the other port j. This, in conjunction with theorem 1, constitutes the proof.

Theorem 8. The C^1 submatrices of the modified cut-set matrices of all n-port networks having identical port configurations, edge and port orientations and potential factors are equal if the submatrices have identical row and column orderings.

Proof. From theorem 1, every entry of C^1 equals the voltage across a particular edge under appropriate excitation conditions. This voltage can be expressed in terms of potential factors in the same way for all n-port networks which have identical port configurations and identical orientations for ports and edges. Since these potential factors are the same for all the networks considered, it follows that all the associated C^1 submatrices are also the same.

Theorem 9. Given the submatrix C^1 of the modified cut-set matrix C of an n-port network with specified edge and port orientations, the potential factors are uniquely determined.

Proof. The proof of the theorem follows from theorem 7.

3 Parallel connection of n-port networks

Consider two n-port networks N_1 and N_2 with Y_1 and Y_2 as their short-circuit admittance matrices. By the parallel connection of the two networks, it is implied that the positive reference terminal of every port in N_1 is connected to the positive reference terminal of the corresponding port in N_2, and similarly for the negative reference terminals. The internal vertexes are left unconnected. If the parallel combination of N_1 and N_2 has a short-circuit admittance matrix Y equal to $Y_1 + Y_2$, we shall refer to it as a proper parallel

connection of N_1 and N_2. If K and K' are the matrices of potential factors of N_1 and N_2, we have, on extending the well known criterion for the proper parallel connection of two 2-port networks, that a sufficient condition for the proper parallel connection of N_1 and N_2 is that $K = K'$. This can also be shown to be necessary if positive R, L and C elements only are permitted.[7] In the following, we assume this to be the case whenever this necessary condition is used.

We now proceed to give an alternative criterion for the proper parallel connection of two n-port networks N_1 and N_2. We first prove a preliminary theorem.

Theorem 10. For a proper parallel connection of N_1 and N_2, it is necessary that the number of external vertexes v_1 of both networks be the same.

Proof. Consider the subgraph of N_1 consisting of only the edges shunting the ports. This subgraph may be in more than one part, but it has no circuit. Now consider any two ports i and j in the network N_1. In the subgraph under consideration, port j may be connected to port i through the positive reference terminal of the latter, or port j may be connected to port i through the negative reference terminal of the latter, or no path may exist between ports j and i. The potential factor K_{ij} is then 1, 0 or $x(x \neq 1, x \neq 0)$, respectively, depending on the port configuration. Since, for a proper parallel connection, the potential factors of N_1 and N_2 must be identical, it is clear that the configuration of ports i and j in N_1 and N_2 must be alike. Since this is true for every pair of ports i and j, we conclude that the subgraph of the edges shunting the ports (the port configuration) must be identical in both networks. It follows from this that the number of external vertexes v_1 in both networks should be the same.

Let C_{N1} and C_{N2} be the modified cut-set matrices of the two networks and C^1_{N1} and C^1_{N2} be the submatrices corresponding to the edges in the complete graph formed by the external vertexes in each network. An edge in one of the two networks is said to correspond to an edge in the other network, if, in the process of paralleling the two networks, the two edges come in parallel. Let C^1_{N1} and C^1_{N2} be so formed that two corresponding ports and edges have, respectively, the same row and column positions. We now give a new criterion for the proper parallel connection of N_1 and N_2.

*Theorem 11.** A sufficient condition for the proper parallel connection of two n-port networks N_1 and N_2 is that the submatrices C^1_{N1} and C^1_{N2} of the modified cut-set matrix of the two networks are equal if the ports and edges are similarly oriented. This is also necessary if positive *RLC* elements only are permitted.

Proof

Sufficiency. From theorem 9, it follows that, if $C^1_{N1} = C^1_{N2}$, the potential factor matrices K and K' are equal. Hence a proper parallel connection of N_1 and N_2 can be made.

Necessity. If a proper parallel connection is possible, the two networks have the same number of external vertexes and the same port configuration. Furthermore, $K = K'$. Therefore, from theorem 8, it follows that C^1_{N1} and C^1_{N2} are equal, which proves the theorem.

It may be observed here that, if two networks can be properly connected in parallel but the orientations of two corresponding edges do not match, the entries in the corresponding columns of C^1_{N1} and C^1_{N2} are equal in magnitude but opposite in sign. In such cases, it is obvious that the two submatrices C^1_{N1} and C^1_{N2} can be made equal by a change in the orientation of one of the edges.

4 Generation of equivalent n-port networks

In connection with the realisation of a given Y matrix, Cederbaum[2] proposed a method of generating equivalent n-port networks for a given n-port network, making use of the modified cut-set matrix C. It was subsequently shown by the authors that Cederbaum's procedure in the form given by him can lead to an equivalent network only if the modified cut-set matrices of the original and the incremental networks are the same. With this modification, the generation of equivalents for a class of networks was discussed in References 3 and 4. In this Section, we give an extension of this procedure applicable to a more general case.

Let an n-port network N_1 having Y_{e1} as its diagonal edge-admittance matrix be given. Let $C = [C^1|C^2]$ be the modified cut-set matrix of N_1. From theorems 6 and 4, any diagonal matrix Y_{e2} satisfying the equations

$$CY_{e2}C_2' = 0 \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (14)$$

and $$CY_{e2}C_1' = 0 \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (15)$$

represents the edge-admittance matrix of an n-port network N_2 having its modified cut-set matrix equal to C and its short-circuit admittance matrix identically equal to zero. It is also seen that a new network N_3, obtained by putting every edge of N_1 in parallel with the corresponding edge of N_2, has the following properties:

(*a*) $Y_{e3} = Y_{e1} + Y_{e2}$, where Y_{e3} is the edge-admittance matrix of N_3.

(*b*) the modified cut-set matrix of N_3 is equal to the modified cut-set matrix C of N_1 by theorem 6, since

$$CY_{e3}C_2' = C(Y_{e1} + Y_{e2})C_2' = CY_{e1}C_2' + CY_{e2}C_2' = 0$$

(*c*) The short-circuit admittance matrix Y_3 of N_3 is the same as the short-circuit admittance matrix Y_1 of N_1, since

$$Y_3 = CY_{e3}C_1' = C(Y_{e1} + Y_{e2})C_1' = CY_{e1}C_1' + CY_{e2}C_1' = Y_1 + 0 = Y_1$$

Thus, for every diagonal admittance matrix Y_{e2} which satisfies eqns. 14 and 15, an equivalent network N_3, having the same short-circuit admittance matrix as N_1, can be generated. It is to be noted that, in this procedure, no distinction is made between internal and external vertexes.

If, however, it is desired to have N_2 with v_1 external vertexes corresponding to those of N_1 and no internal vertex, the following equations have to be solved:

$$C^1Y_{e2}(C^1_{2a})' = 0 \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (16)$$

$$C^1Y_{e2}(C^1_1)' = 0 \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (17)$$

where C^1 and C^1_1 are the submatrices of C and C_1 corresponding to the $\frac{1}{2}v_1(v_1 - 1)$ edges in the complete graph formed on the v_1 external vertexes, and C^1_1 and C^1_{2a} together form a fundamental cut-set matrix of this complete graph. From the discussion in Section 3 it is clear that, by joining the corresponding pairs of external vertexes of N_1 and N_2, a proper parallel connection is obtained, yielding an n-port network N_3 having its short-circuit admittance matrix equal to that of N_1. In this case, Y_{e2} is a diagonal matrix of order $\frac{1}{2}v_1(v_1 - 1)$.

For a proper realisation of Y_1, each entry in the edge-admittance matrix Y_{e3} of N_3 in either of these procedures should be a positive real function. This restriction, however, does not apply to Y_{e2}. While the results of this Section are generally valid, it is difficult to apply them directly to generate

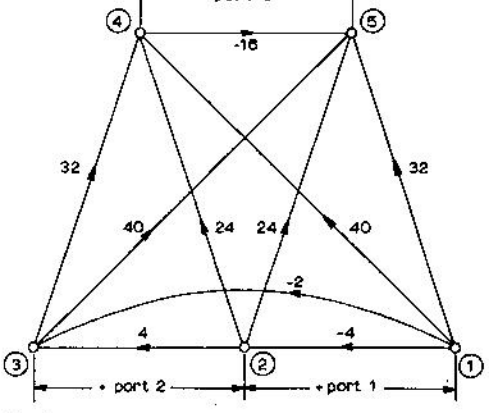

Fig. 1

Given 3-port network with some negative conductances

* A similar condition was obtained recently for the special case of networks containing no internal vertexes.[8]

equivalent *RLC* networks. However, in a separate paper[9] the usefulness of these results in the synthesis of 2-element-kind n-port networks is demonstrated. For the resistive n-port-network case, however, the results can be conveniently used to generate a class of continuously equivalent networks.[10] The following example serves to illustrate the procedure.

Consider the 3-port network given in Fig. 1 and having the following short-circuit admittance matrix Y:

$$Y = \begin{bmatrix} 39 & 25 & -4 \\ 25 & 47 & -4 \\ -4 & -4 & 32 \end{bmatrix}$$

The network contains negative resistances, and we wish to generate an equivalent network with all positive elements. Adopting the convention that the column headed by ij refers to the edge joining vertices i and j, and choosing the tree constituted by 12, 23, 34 and 45, we have

$$\begin{array}{c} \\ C_1 = \\ \\ C_2 = \\ \\ C = \frac{1}{8} \end{array} \begin{array}{c} \begin{array}{cccccccccc} 12 & 13 & 14 & 15 & 23 & 24 & 25 & 34 & 35 & 45 \end{array} \\ \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \\ \begin{bmatrix} 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 0 \end{bmatrix} \\ \begin{bmatrix} 8 & 8 & 5 & 5 & 0 & -3 & -3 & -3 & -3 & 0 \\ 0 & 8 & 3 & 3 & 8 & 3 & 3 & -5 & -5 & 0 \\ 0 & 0 & -4 & 4 & 0 & -4 & 4 & -4 & 4 & 8 \end{bmatrix} \end{array}$$

To generate an equivalent 3-port network, we seek a network N_2 satisfying eqns. 14 and 15. If the column matrix y_{e2} represents the edge conductances in this network, with its rows ordered to correspond to edges in the same way as the columns of C, C_1 and C_2, the two equations can be put in the following form, after taking the symmetry of the matrix $CY_{e2}C_1'$ into account:

$$\begin{bmatrix} 0 & 0 & 5 & 5 & 0 & -3 & -3 & -3 & -3 & 0 \\ 0 & 0 & 3 & 3 & 0 & 3 & 3 & -5 & -5 & 0 \\ 0 & 0 & -4 & 4 & 0 & -4 & 4 & -4 & 4 & 0 \end{bmatrix} y_{e2} = 0$$

$$\begin{bmatrix} 8 & 8 & 5 & 5 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 8 & 5 & 5 & 0 & -3 & -3 & 0 & 0 & 0 \\ 0 & 0 & 0 & 5 & 0 & 0 & -3 & 0 & -3 & 0 \\ 0 & 8 & 3 & 3 & 8 & 3 & 3 & 0 & 0 & 0 \\ 0 & 0 & 0 & 3 & 0 & 0 & 3 & 0 & -5 & 0 \\ 0 & 0 & 0 & 4 & 0 & 0 & 4 & 0 & 4 & 8 \end{bmatrix} y_{e2} = 0$$

There are nine equations in ten unknowns, and hence a solution can be found taking an arbitrary value for one of the unknowns. Hence a range of continuously equivalent networks can be found by varying the value of this unknown in a continuous manner. A particular solution for y_{e2} is

$$y_{e2} = \begin{bmatrix} 12 \\ 18 \\ -24 \\ -24 \\ 12 \\ -16 \\ -16 \\ -24 \\ -24 \\ 32 \end{bmatrix}$$

The network N_3 obtained by putting this network N_2 in parallel with N_1 is shown in Fig. 2.

If we now wish to generate another network equivalent to the network shown in Fig. 2, we can seek another solution of the same set of equations as above, to represent the incremental conductances. A possible solution y_{e2} in this case is

$$y_{e2} = \begin{bmatrix} -4 \\ -6 \\ 8 \\ 8 \\ -4 \\ 16/3 \\ 16/3 \\ 8 \\ 8 \\ -32/3 \end{bmatrix}$$

When the conductances in Fig. 2 are increased by these amounts, the equivalent network shown in Fig. 3 results.

This example illustrates the technique of equivalent-network generation. It also illustrates the possibility of generating

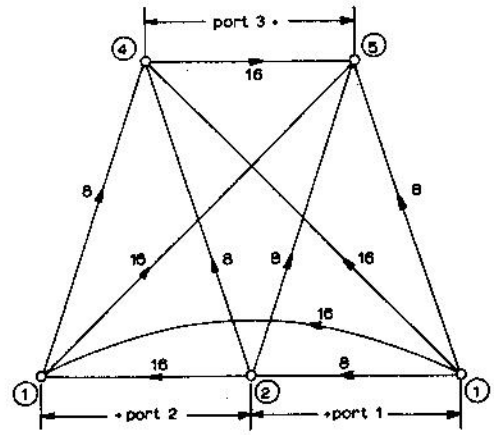

Fig. 2
Equivalent 3-port network for network in Fig. 1

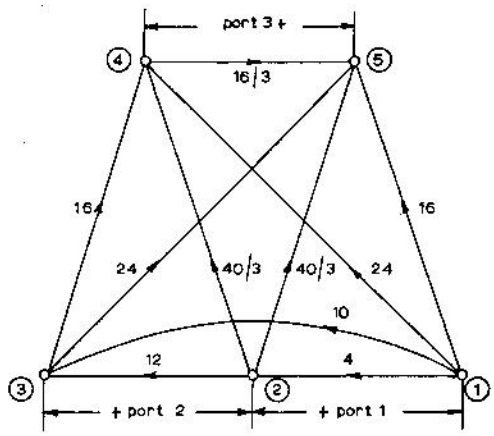

Fig. 3
Another 3-port network equivalent to networks of Figs. 1 and 2

equivalent networks with all nonnegative conductances from one with some negative conductances. For an n-port network with $v > n + 1$, it can be shown that the number of independent equations represented by eqns. 14 and 15 is always less than the number of unknowns, and the flexibility of choosing one or more incremental conductances arbitrarily is always available. It may be noted that the class of networks obtained by this method is characterised by the property that all networks belonging to this class have the same modified cut-set matrix. It is also seen that, using this method, a large number of continuously equivalent networks containing only positive resistances can always be obtained for a resistive n-port network in which every pair of vertexes is connected by a finite positive resistance.

5 Conclusion

It is shown that the modified cut-set matrix of an n-port network which is a generalisation of the conventional cut-set matrix of graph theory has many interesting and significant properties in connection with the analysis of n-port networks. Some of these properties have been used to establish a new criterion for the proper parallel connection of two n-port networks. In the synthesis of *RLC* n-port networks by the parallel connection of a resistive network, an inductive network and a capacitive network, or by the parallel connection of networks realising the residue matrices, such a test is useful. This new criterion requires, for the network under test, the inversion of a square matrix of order $v - n - 1$ for the

determination of C, whereas the conventional method of the determination of potential factors by node analysis requires the inversion of n such matrices.

The methods of Section 4 enable the generation of a range of continuously equivalent n-port networks for a given n-port network, particularly for resistive n-port networks. This would be advantageous in situations where one or more conductances of the network to be realised are required to have some initially specified values. This procedure is also potentially useful in the general n-port-network synthesis problem, in that, starting from any realisation with some negative conductances, one may seek a proper realisation through the equivalent-network approach.

6 Acknowledgment

This work forms part of a doctoral thesis submitted by one of the authors (K. T.) to the Indian Institute of Technology, Madras.

7 References

1 SESHU, S., and REED, M. B.: 'Linear graphs and electrical networks (Addison Wesley, 1961)
2 CEDERBAUM, I.: 'On equivalence of resistive n-port networks', *IEEE Trans.*, 1965, **CT–12**, pp. 338–344
3 THULASIRAMAN, K., and MURTI, V. G. K.: 'Comment on "On equivalence of resistive n-port networks"', *ibid.*, 1967, **CT–14**, pp. 357–359
4 MURTI, V. G. K., and THULASIRAMAN, K.: 'Synthesis of a class of n-port networks', *ibid.*, 1968, **CT–15**, pp. 54–63
5 MURTI, V. G. K., and THULASIRAMAN, K.: 'Parallel connection of n-port networks', *Proc. Inst. Elect. Electronics Engrs.*, 1967, **55**, pp. 1216–1217
6 GUILLEMIN, E. A.: 'On the realisation of an nth order G-matrix', *IEEE Trans.*, 1961, **CT–8**, pp. 318–323
7 THULASIRAMAN, K.: 'The modified cut-set and circuit matrices and synthesis of n-port networks', Ph.D. thesis, Department of Electrical Engineering, Indian Institute of Technology, Madras, Dec. 1967
8 CEDERBAUM, I.: 'Parallel interconnection of n-port networks', *IEEE Trans.*, 1967, **CT–14**, pp. 274–279
9 THULASIRAMAN, K., and MURTI, V. G. K.: 'Synthesis applications of the modified cut-set matrix', see pp. 1269–1274
10 CALAHAN, D. A.: 'Modern network synthesis', Vol. 2 (Hayden, New York, 1964)