Circuit Theory

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CIRCUIT THEORY is an important and perhaps the oldest branch of electrical engineering. A circuit is an interconnection of electrical elements: passive elements such as resistances, capacitances, inductances, active elements, and sources (or excitations). Two variables—namely, voltage and current variables—are associated with each circuit element. There are two aspects to circuit theory: analysis and design. In circuit analysis, we are interested in determination of the values of currents and voltages in different elements of the circuit, given the values of the sources or excitations. On the other hand, in circuit design, we are interested in the design of circuits, which exhibit certain prespecified voltage or current charactersitics at one or more parts of the circuit. In this chapter, we will confine our discussion to certain aspects of circuit analysis.

The behavior or dynamics of a circuit is described by three systems of equations determined by Ohm's law, Kirchhoff's voltage law, and Kirchhoff's current law. Ohm's law specifies the relationship between the voltage and current variables associated with a circuit element. This relationship is not specified for independent sources. Also, this relationship could be linear or nonlinear. If the relationship is linear, then the circuit element is called a *linear element*; otherwise, it is called a *nonlinear element*. A circuit is linear if it contains only linear elements besides independent sources. Kirchhoff's voltage specifies the dependence among the voltage variables in the circuit, and Kirchhoff's current law specifies the dependence among the current variables in the circuit.

The systems of equations determined by the application of Kirchhoff's voltage and current laws depend on the structure or the graph of the circuit. In other words, they depend only on the way the circuit elements are interconnected. Thus, the graph of a circuit plays a fundamental role in the study of circuits. Several interesting properties of circuits depend only on the structure of the circuits. Thus, the theory of graphs has played a fundamental role in discovering structural properties of electrical circuits.

In this chapter we shall develop most of those results that form the foundation of graph theoretic study of electrical circuits. A comprehensive treatment of these developments may be found in Swamy and Thulasiraman (1981). All theorems in this chapter are stated without proofs. Our discussion here follows closely our development in the Graph Theoretic Foundation of Circuit Analysis chapter in Chen (2001).

I. GRAPH THEORY: BASIC CONCEPTS AND RESULTS

Our development of graph theory is self-contained, except for the definitions of standard and elementary results from set theory and matrix theory.

• **Graph:** A graph $G = (V, E)$ consists of two sets, a finite set $V = (v1, v_2, \ldots, v_n)$ of elements called *vertices* and a finite set $E = (e_1, e_2, \ldots, e_n)$ of elements called *edges*.

• **Directed and undirected graph:** If the edges of G are identified with ordered pairs of vertices, then G is called a directed or an *oriented graph*; otherwise, it is called an *undirected* or an *unoriented graph*.

Graphs permit easy pictorial representations. In a pictorial representation each vertex is represented by a dot and each edge is represented by a line joining the dots associated with the edge. In directed graphs, an orientation or direction is assigned to each edge. If the edge is associated with the ordered pair (v_i, v_j), then this edge is oriented from v_i to v_j. If an edge e connects vertices v_i and v_j, then it is denoted by $e = (v_i, v_j)$. In a directed graph, (v_i, v_j) refers to an edge directed from (v_i, v_j). A graph and a directed graph are shown in Fig. 1. Unless explicitly stated, the term "graph" may refer to a directed graph or an undirected graph.

• **End vertices:** The vertices v_i and v_j associated with an edge are called the *end vertices* of the edge.

• **Parallel edges:** All edges having the same pair of end vertices are called *parallel* edges. In a directed graph parallel edges refer to edges connecting the same pair of verices v_i and v_j the same way from v_i to v_j or from v_j to v_i. For instance, in the graph of Fig. 1a, the edges connecting v_1 and v_2 are parallel edges. In the directed graph of Fig. 1b the edges connecting v_3 and v_4 are parallel edges. However, the edges connecting v_1 and v_2 are not parallel edges because they are not oriented in the same way.

• **Self loop:** If the end vertices of an edge are not distinct, then the edge is called a *self loop*. The graph of Fig. 1a has one self loop and the graph of Fig. 1b has two self loops.
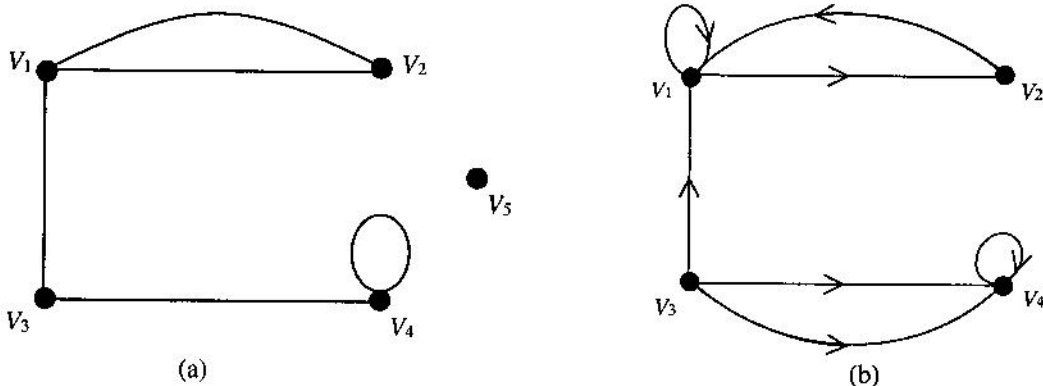
An edge is said to be *incident on* its end vertices. In a directed graph the edge (v_i, v_j) is said to be *incident out* of v_i and is said to be *incident into* v_j. Vertices v_i and v_j are adjacent if an edge connects v_i and v_j.

• **Degee:** The number of edges incident on a vertex v_i is called the *degree* of v_i and is denoted by $d(v_i)$.

• **In-degree:** In a directed graph, $d_{in}(v_i)$ refers to the number of edges incident into vertex v_i, and it is called the *in-degree*.

• **Out-degree:** In a directed graph, $d_{out}(v_i)$ refers to the number of edges incident out of the vertex v_i.

• **Isolated vertex:** If $d(v_i) = 0$, then v_i is said to be an *isolated vertex*.

• **Pendant vertex:** If $d(v_i) = 1$, then v_i is said to be a *pendant vertex*.

A self loop at a vertex v_i is counted twice while computing $d(v_i)$. As an example, in the graph of Fig. 1a, $d(v_1) = 3$, $d(v_4) = 3$, and v_5 is an isolated vertex. In the directed graph of Fig. 1b, $d_{in}(v_1) = 3$, and $d_{out}(v_1) = 2$.

Note that in a directed graph, for every vertex v_i,

$$d(v_i) = d_{in}(v_i) + d_{out}(v_i)$$

Theorem 1

1. The sum of the degrees of the vertices of a graph G is equal to $2m$, where m is the number of edges of G.

2. In a directed graph with m edges, the sum of the in-degrees and the sum of the out-degrees are both equal to m.

The following theorem is known to be the first major result in graph theory.

Theorem 2

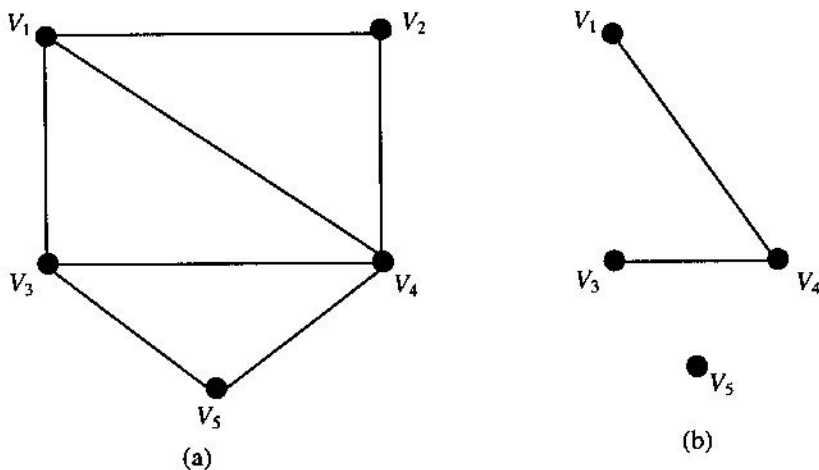*The number of vertices of odd degree in any graph is even.*

FIGURE 1 (a) An undirected graph, (b) a directed graph.

FIGURE 2 (a) Graph G; (b) subgraph G.

Consider a graph $G = (V', E')$. The graph $G' = (V', E')$ is a subgraph of G if $V' \subseteq V$ and $E' \subseteq E$. As an example, a graph G and a subgraph of G are shown in Fig. 2.

- **Path:** In a graph G a *path* P connecting vertices v_i and v_j is an alternating sequence of vertices and edges starting at v_i and ending at v_j, with all vertices except v_i and v_j being distinct.
- **Directed path:** In a directed graph a path P connecting vertices v_i and v_j is a called a *directed path* from v_i to v_j if all the edges in P are oriented in the same direction as we traverse P from v_i toward v_j.
- **Circuit:** If a path starts and ends at the same vertex, it is called a *circuit*.
- **Directed circuit:** In a directed graph, a circuit in which all the edges are oriented in the same direction is called a *directed circuit*. It is often convenient to represent paths and circuits by the sequence of edges representing them. For example, in the undirected graph of Fig. 3a, P: e_1, e_2, e_3, e_4 is a path connecting v_1 and v_5,

and C: $e_1, e_2, e_3, e_4, e_5, e_6$ is a circuit. In the directed graph of Fig. 3b, P: e_1, e_2, e_7, e_5 is a directed path, and C: e_1, e_2, e_7, e_6 is a directed circuit. Note that C: e_7, e_5, e_4, e_1, e_2 is a circuit in this directed graph, although it is not a directed circuit. Similarly, P: e_9, e_6, e_1 is a path but not a directed path.

- **Connected graph:** A graph is *connected* if there is a path between every pair of vertices in the graph; otherwise, the graph is not connected. For example, the graph in Fig. 2a is a connected graph, whereas the graph in Fig. 2b is not a connected graph.
- **Tree:** A *tree* is a graph that is connected and has no circuits.
- **Spanning tree:** Consider a connected graph G, A subgraph of G is a *spanning tree* of G if the subgraph is a tree and contains all the vertices of G. A tree and a spanning tree of the graph of Fig. 4a are shown in Figs. 4b and 4c, respectively.
- **Branches:** The edges of a spanning tree T are called the braches of T.
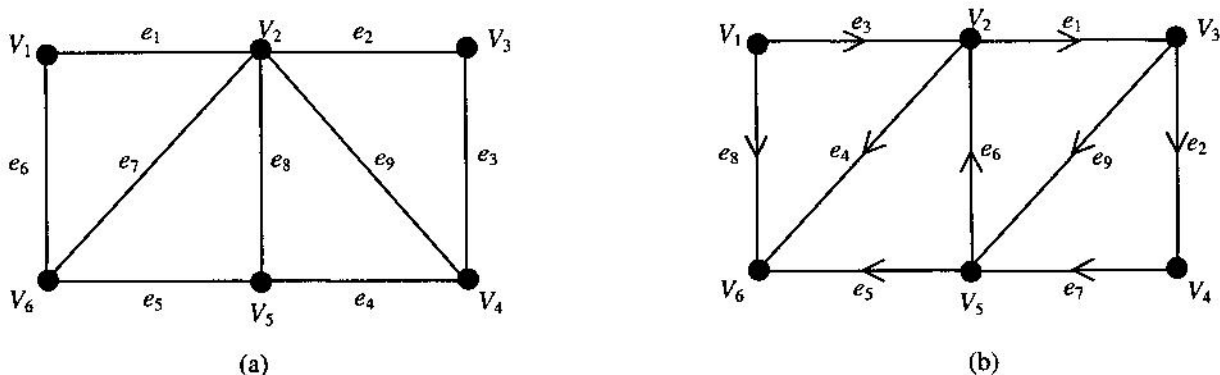

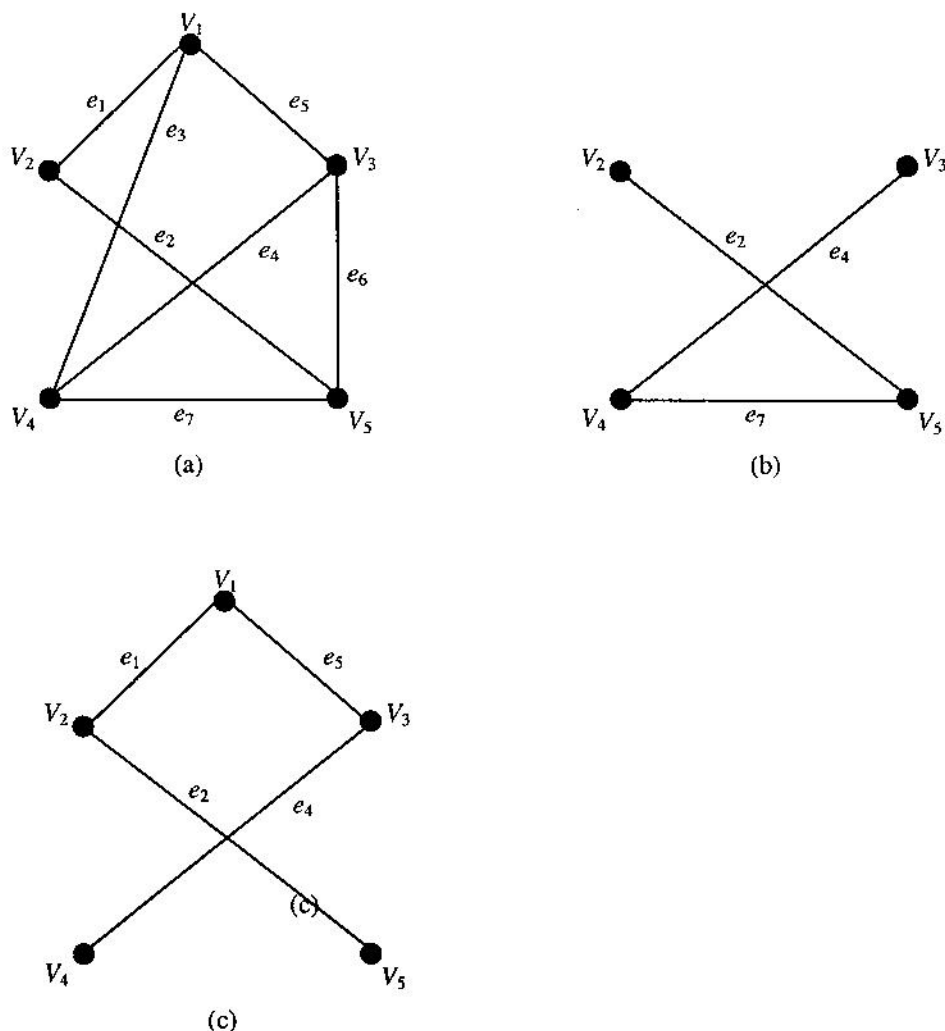**FIGURE 3** (a) An undirected graph; (b) a directed graph.

FIGURE 4 (a) Graph G; (b) a tree of graph G; (c) a spanning tree of G.

• **Cospanning tree:** Given a spanning tree of connected graph G, the cospanning tree relative to T is the subgraph of G induced by the edges that are not present in T. For example, the cospanning tree is relative to the spanning tree T if Fig. 4c consists of the edges e_3, e_6, e_7.

• **Chords:** The edges of a cospanning tree are called *chords*.

It can be easily be verified that in a tree exactly one path connects any two vertices. It should be noted that a tree is minimally connected in the sense that removing any edge from the tree will result in a disconnected graph.

Theorem 3

A tree on n vertices has $n - 1$ edges.

If a connected graph G has n vertices and m edges, then the rank ρ and nullity μ of G are defined as follows:

$$\rho(G) = n - 1$$
$$\mu(G) = m - n + 1$$

The concepts of rank and nullity have parallels in other branches of mathematics, such as matrix theory.

Clearly, if G is connected, then any spanning tree of G has $\rho = n - 1$ branches and $\mu = m - n + 1$ chords.

A. Cuts, Circuits, and Orthogonality

We introduce here the notions of a cut and a cutset and develop certain results which bring out the dual nature of circuits and cutsets. Consider a connected graph $G = (V, E)$ with n vertices and m edges. Let V_1 and V_2 be two mutually disjoint nonempty subsets of V such that $V = V_1 \cup V_2$; thus, V_2 is the complement of V_1 in V and vice versa. V_1 and V_2 are also said to form a partition of V. Then the set
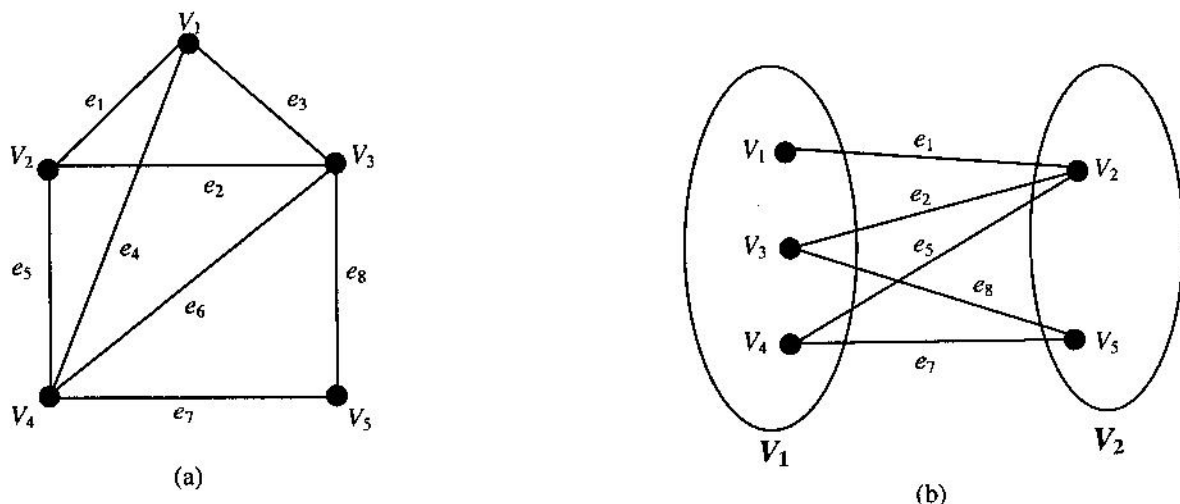
FIGURE 5   (a) Graph G; (b) cut $\langle V_1, V_2 \rangle$ of G.

of all those edges which have one end vertex in V_1 and the other in V_2 is called a *cut* of G. As an example, a graph and a cut $\langle V_1, V_2 \rangle$ of G are shown in Fig. 5.

The graph G' which results after removing the edges in a cut will not be connected. A *cutset S* of a connected graph G is a minimal set of edges of G such that removal of S disconnects G. Thus, a cutset is also a cut. Note that the minimality property of a cutset implies that no proper subset of a cutset is a cutset.

Consider a spanning tree T of a connected graph G. Let b be a branch of T. Removal of the branch b disconnects T into two trees, T_1 and T_2. Let V_1 and V_2 denote the vertex sets of T_1 and T_2, respectively. Note that V_1 and V_2 together contain all the vertices of G. We can verify that the cut $\langle V_1, V_2 \rangle$ is a cutset of G and is called the *fundamental cutset* of G with respect to branch b of T. Thus, for a given graph G and a spanning tree T of G, we can construct $n - 1$ fundamental cutsets, one for each branch of T. As an example, for the graph shown in Fig. 5, the fundamental cutsets with respect to the spanning tree $T = [e_1, e_2, \ldots, e_6, e_8]$ are

Branch e_1: (e_1, e_3, e_4)
Branch e_2: (e_2, e_3, e_4, e_5)
Branch e_6: (e_6, e_4, e_5, e_7)
Branch e_8: (e_8, e_7)

Note that the fundamental cutset with respect to branch b contains b. Furthermore, branch b is not present in any other fundamental cutset with respect to T.

Next we identify a special class of circuits of a connected graph G. Again, let T be a spanning tree of G. Because exactly one path exists between any two vertices of T, adding a chord c to T produces a unique circuit. This

circuit is called the *fundamental circuit* of G with respect to chord c of T. Note again that the fundamental circuit with respect to chord c contains c, and chord C is not present in any other fundamental circuit with respect to T. As an example, the set of fundamental circuits with respect to the spanning tree $T = (e_1, e_2, e_6, e_8)$ of the graph shown in Fig. 5 is

Chord e_3: (e_3, e_1, e_2)
Chord e_4: (e_4, e_1, e_2, e_6)
Chord e_5: (e_5, e_2, e_6)
Chord e_7: (e_7, e_8, e_6)

B. Incidence, Circuit, and Cut Matrices of a Graph

The incidence, circuit, and cut matrices are coefficient matrices of Kirchoff's equations which describe an electrical network. We next define these matrices and present some properties of these matrices which are useful in the study of electrical networks.

1. Incidence Matrix

Consider a connected directed graph G with n vertices and m edges and having no self loops. The *all-vertex incidence matrix* $A_c = [a_{ij}]$ of G has n rows, one for each vertex, and m columns, one for each edge. The element a_{ij} of A_c is defined as follows:

$$a_{ij} = \begin{cases} 1, & \text{if } j\text{th edge is incident out of the } i\text{th vertex} \\ -1, & \text{if } j\text{th edge is incident into the } i\text{th vertex} \\ 0, & \text{if the } j\text{th edge is not incident on the } i\text{th vertex} \end{cases}$$

As an example, the A_c matrix of the directed graph in Fig. 6 is given below:
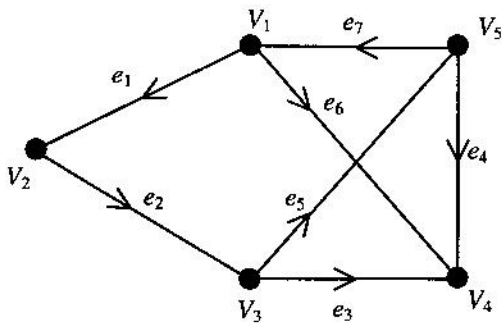
FIGURE 6 A directed graph.

$$
\begin{array}{c c c c c c c c}
 & e_1 & e_2 & e_3 & e_4 & e_5 & e_6 & e_7 \\
v_1 & \begin{bmatrix} 1 \\ -1 \\ 1 \\ 0 \\ 0 \end{bmatrix} & \begin{matrix} 0 \\ 1 \\ -1 \\ 0 \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \\ 1 \\ -1 \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \\ 0 \\ -1 \\ 1 \end{matrix} & \begin{matrix} 0 \\ 0 \\ 1 \\ 0 \\ -1 \end{matrix} & \begin{matrix} 1 \\ 0 \\ 0 \\ -1 \\ 0 \end{matrix} & \begin{matrix} -1 \\ 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}
\end{array}
$$

From the definition of A_c, it should be clear that each column of this matrix has exactly two nonzero entries, one $+1$ and one -1; therefore, we can obtain any row of A_c from the remaining rows. Thus,

$$\operatorname{rank}(A_c) \le n - 1$$

An $(n-1)$-rowed submatrix of A_c is referred to as an *incidence matrix* of G. The vertex which corresponds to the row which is not in A_c is called the *reference vertex* of A.

2. Cut Matrix

Consider a cut (V_a, V_b) in a connected directed graph G with n vertices and m edges. Recall that $\langle V_a, V_b \rangle$ consists of all those edges connecting vertices in V_a to V_b. This cut may be assigned an orientation from V_a to V_b or from V_b to V_a. Suppose the orientation of (V_a, V_b) is from V_a to V_a. Then the orientation of an edge (v_i, v_j) is said to agree with the cut orientation if $v_i \in V_a$, and $v_j \in V_b$.

The *cut matrix* $Q_c = [q_{ij}]$ of G has m columns, one for each edge, and has one row for each cut. The element q_{ij} is defined as follows:

$$
q_{ij} = \begin{cases}
1, & \text{if the } j\text{th edge is in the } i\text{th cut and its} \\
 & \text{orientation agrees with the cut orientation} \\
-1, & \text{if the } j\text{th edge is in the } i\text{th cut and its} \\
 & \text{orientation does not agree} \\
 & \text{with the cut orientation} \\
0, & \text{if the } j\text{th edge is not in the } i\text{th cut}
\end{cases}
$$

Each row of Q_c is called the *cut vector*. The edges incident on a vertex form a cut. Thus it follows that the

matrix A_c is a submatrix of Q_c. Next we identify another important submatrix of Q_c.

Recall that each branch of a spanning tree T of connected graph G defines a fundamental cutset. The submatrix of Q_c corresponding to the $n - 1$ fundamental cutsets defined by T is called the *fundamental cutset matrix Q_f* of G with respect to T.

Let $b_1, b_2, \ldots, b_{n-1}$ denote the branches of T. Let us assume that the orientation of a fundamental cutset is chosen so as to agree with that of the defining branch. Suppose we arrange the rows and the columns of Q_f so that the ith column corresponds to the fundamental cutset defined by b_i. Then the matrix Q_f can be displayed in a convenient form as follows:

$$Q_f = [U \mid Q_{fc}]$$

where U is the unit matrix of order $n - 1$, and its columns correspond to the branches of T. As an example, the fundamental cutset matrix of the graph in Fig. 6 with respect to the spanning tree $T = (e_1, e_2, e_5, e_6)$ is given below:

$$
Q_f = \begin{array}{c c c c c c c c}
 & e_1 & e_2 & e_5 & e_6 & e_3 & e_4 & e_7 \\
e_1 & \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} & \begin{matrix} 0 \\ 1 \\ 0 \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \\ 1 \\ 0 \end{matrix} & \begin{matrix} 0 \\ 0 \\ 0 \\ 1 \end{matrix} & \begin{matrix} -1 \\ -1 \\ 0 \\ 1 \end{matrix} & \begin{matrix} -1 \\ -1 \\ -1 \\ 1 \end{matrix} & \begin{matrix} -1 \\ -1 \\ -1 \\ 0 \end{bmatrix}
\end{array}
$$

It is clear that the rank of Q_f is $n - 1$. Hence,

$$\operatorname{rank}(Q_c) \ge n - 1$$

3. Circuit Matrix

Consider a circuit C in a connected directed graph G with n vertices and m edges. This circuit can be traversed in one of two directions, clockwise or counterclockwise. The direction we choose for traversing C is called the *orientation* of C. If an edge $e = (v_i, v_j)$ directed from v_i to v_j is in C and if v_i appears before v_j as we traverse C in the direction specified by the orientation of C, then we say that the orientation agrees with the orientation of e.

The *circuit matrix* $B_c = [b_{ij}]$ of G has m columns, one for each edge, and has one row for each circuit in G. The element b_{ij} is defined as follows:

$$
b_{ij} = \begin{cases}
1, & \text{if the } j\text{th edge is in the } i\text{th circuit} \\
 & \text{and its orientation agrees} \\
 & \text{with the circuit orientation} \\
-1, & \text{if the } j\text{th edge is in the } i\text{th circuit} \\
 & \text{and its orientation does not agree} \\
 & \text{with circuit orientation} \\
0, & \text{if the } j\text{th edge is not in the } i\text{th circuit}
\end{cases}
$$

The submatrix of B_c corresponding to the fundamental circuits defined by the chords of a spanning tree T is called

the *fundamental circuit matrix* B_f of G with respect to the spanning tree T.

Let $c_1, c_2, c_3, \ldots, c_{m-n+1}$ denote the chords of T. Suppose we arrange the columns and the rows of B_f so that the ith row corresponds to the fundamental circuit defined by the chord c_i and the ith column corresponds to the chord c_i. If, in addition, we choose the orientation of a fundamental circuit to agree with the orientation of the defining chord, we can write B_f as:

$$B_f = [U \perp B_{ft}]$$

where U is the unit matrix of order $m - n + 1$, and its columns correspond to the chords of T.

As an example, the fundamental circuit matrix of the graph shown in Fig. 6 with respect to the tree $T = (e_1, e_2, e_5, e_6)$ is given below:

$$B_f = \begin{array}{c} \\ e_3 \\ e_4 \\ e_7 \end{array} \begin{array}{c} e_3 \ \ e_4 \ \ e_7 \ \ e_1 \ \ e_2 \ \ e_5 \ \ e_6 \\ \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 0 & -1 \\ 0 & 1 & 0 & 1 & 1 & 1 & -1 \\ 0 & 0 & 1 & 1 & 1 & 1 & 0 \end{bmatrix} \end{array}$$

It is clear from the above that the rank of B_f is $m - n + 1$; hence,

$$\text{rank}(B_c) \geq m - n + 1.$$

The following results constitute the foundation of the graph theoretic application to electrical circuit analysis.

Theorem 4 (orthogonality relationship)

1. A circuit and a cutset in a connected graph have an even number of common edges.

2. If circuit and a cutset in a directed graph have $2k$ common edges, then k of these edges have the same relative orientation in the circuit and the cutset, and the remaining k edges have one orientation in the circuit and the oppostite orientation in the cutset.

Theorem 5

If the columns of the circuit matrix B_c and the columns of the cut matrix Q_c are arranged in the same edge order, then

$$B_c Q_c = 0$$

Theorem 6

Rank$(B_c) = m - n + 1$ and rank$(Q_c) = n - 1$.

Note that it follows from the above theorem that the rank of the circuit matrix is equal to the nullity of the graph, and the rank of the cut matrix is equal to the rank of the graph. This result, in fact, motivated the definitions of the rank and nullity of a graph
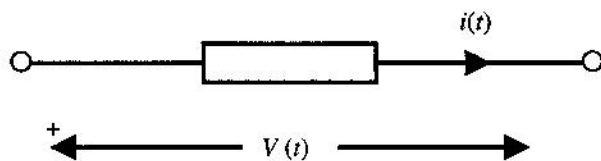

FIGURE 7 A network element with reference convention.

II. GRAPHS AND ELECTRICAL NETWORKS

An electrical network is an interconnection of electrical network elements such as resistances, capacitances, inductances, voltage and current sources, etc. Each network element is associated with two variables, the voltage variable, $v(t)$ and the current variable $i(t)$. We also assign reference directions to the network elements (see Fig. 7) so that $i(t)$ is positive whenever the current is in the direction of the arrow, and $v(t)$ is positive whenever the voltage drop in the network element is in the direction of the arrow. Replacing each element and its associated reference direction by a directed edge results in the directed graph representing the network. For example, a simple electrical network and the corresponding directed graph are shown in Fig. 8.

The physical relationship between the current and voltage variables of network elements is specified by Ohm's law. For voltage and current sources, the voltage and current variables are required to have specified values. The linear dependence among the voltage variables in the network and the linear dependence among the current variables are governed by Kirchoff's voltage and current laws.

Kirchoff's Voltage Law (KVL): The algebraic sum of the voltages around any circuit is equal to zero.

Kirchoff's Current Law (KCL): The algebraic sum of the currents flowing out of a node is equal to zero.

As an example, the KVL equation for the circuit 1, 3, 5 and the KCL equation for vertex b in the graph of Fig. 8 and

Circuit 1, 3, 5 $\quad v_1 + v_3 + v_5 = 0$

Vertex b $\quad -i_1 + i_2 + i_3 = 0$

It can be easily seen that KVL and KCL equations for an electrical network N can be conveniently written as:

$$A_c I_e = 0$$

and

$$B_c V_e = 0$$

where A_c and B_c are, respectively, the incidence and circuit matrices of the directed graph representing N; I_e and V_e are, respectively, the column vectors of element currents and voltages in N. Because each row in the cut matrix Q_c can be expressed as a linear combination of the rows of
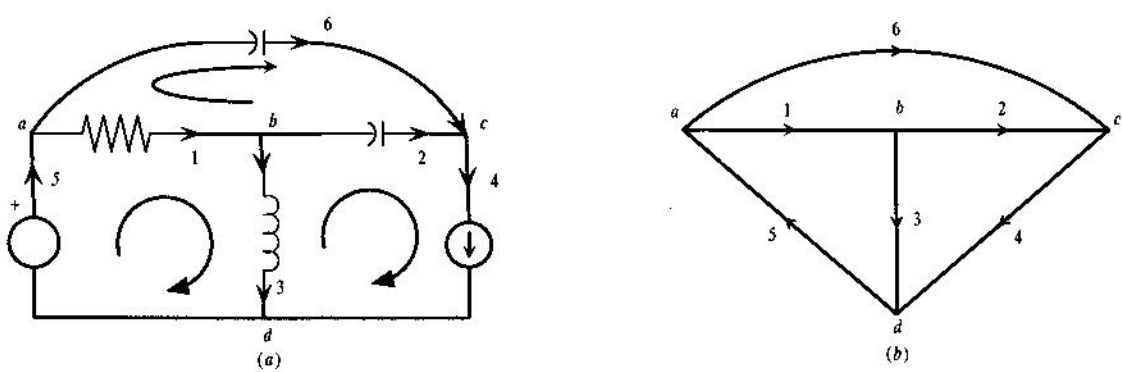
FIGURE 8 (a) An electrical network N; (b) directed graph representation of N.

the matrix, in the above we can replace A_c by Q_c; thus, we have

$$\text{KCL:} \quad Q_c I_e = 0$$
$$\text{KVL:} \quad B_c V_e = 0$$

Thus, KCL can also be stated as: The algebraic sum of the currents in any cut of N is equal to zero.

If a network N has n vertices and m elements and its graph is connected, then there are only $(n-1)$ linearly independent cuts and only $(m - n + 1)$ linearly independent circuits. Thus, in writing KVL and KCL equations we need to use only B_f, a fundamental circuit matrix, and Q_f, a fundamental circuit matrix, respectively. Thus, we have

$$\text{KCL:} \quad Q_f I_e = 0$$
$$\text{KVL:} \quad B_f V_e = 0$$

We note that the KCL and KVL equations depend only on the way network elements are interconnected and not on the nature of the network elements. Thus, several results in electrical network theory are essentially graph theoretic in nature. Some results of interest in electrical network analysis are presented in the reminder of this chapter. In the following, a network N and its directed graph representation are both denoted by N.

Loop and Cutset Transformations

Let T be a spanning tree of an electrical network. Let I_c and V_t be the column vectors of chord currents and branch currents with respect to T.

1. Loop transformation:

$$I_e = B_f^t I_c$$

2. Cutset transformation:

$$V_e = Q_f^t V_t$$

If, in the cutset transformation, we replace Q_f by the reduced incidence matrix A, then we get the *node transformation* given below:

$$V_e = A^t V_n$$

where the elements in the vector V_n can be interpreted as the voltages of the nodes with respect to the reference node r. (Note: the matrix A does not contain the row corresponding to the node r.)

The above transformations have been extensively employed in developing different methods of network analysis. Two of these methods are described in the following.

III. LOOP AND CUTSET SYSTEMS OF EQUATIONS

As we observed earlier, the problem of network analysis is to determine the voltages and currents associated with the elements of an electrical network. These voltages and currents can be determined from Kirchoff's equations and the element voltage–current (in short, $v - i$) relations given by Ohm's law. However, these equations involve a a large number of variables. As can be seen from the loop and cutset transformations, not all these variables are independent Furthermore, in place of KCL equations we can use the loop transformation which invloves only chord currents as variables. Similarly, KVL equations can be replaced by the cutset transformation which involves only branch voltage variables. We can take advantage of these transformations to establish different sytems of network equations known as the loop and cutset systems.

In deriving the loop system we use the loop transformation in place of KCL, and in this case the loop variables (chord currents) will serve as independent variables. In deriving the cutset system we use the cutset transformation in place of KVL, and the cutset variables (tree branch voltages) will serve as the independent variables in this case. Consider a connected electrical network N. We assume that N consists of only resistances (R), capacitances (C), inductances (L) (referred to collectively as RCL) including mutual inductances, and independent

voltage and current sources. We also assume that all initial inductor currents and initial capacitor volatages have been replaced by appropriate sources. Further, the volatage and current variables are all Laplace transforms of the complex frequency variable s. In N there can be no circuit consisting of only independent voltage sources, for, if such a circuit of sources were present, then by KVL there would be a linear relationship among the corresponding voltages, violating the independence of the voltage sources. For the same reason, in N there can be no cutset consisting of only independent current sources. So there exists in N a spanning tree containing all the voltage sources but not current sources. Such a tree is the starting point for the development of both the loop and cutset systems of equations.

Let T be a spanning tree of the given network such that T contains all the voltage sources but no current sources. Let us partition the element voltage V_e and the element current vector I_e as follows:

$$V_e = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \quad \text{and} \quad I_e = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}$$

where the subscripts 1, 2, and 3 refer to the vectors corresponding to the current sources, RCL elements, and voltage sources, respectively. Let B_f be the fundamental circuit matrix of N, and Q_f the fundamental cutset matrix of N with respect to T. Then the KVL and the KCL equations can written as follows:

$$\text{KVL:} \quad B_f V_e = \begin{bmatrix} U & B_{12} & B_{13} \\ 0 & B_{22} & B_{23} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = 0$$

$$\text{KCL:} \quad Q_f I_e = \begin{bmatrix} Q_{11} & Q_{12} & 0 \\ Q_{21} & Q_{22} & U \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = 0$$

A. Loop Method of Network Analysis

- Step 1: Solve the following for the vector I_l (note that I_l is the vector of currents in the nonsource chords of T).

$$Z_l I_l = -B_{23} V_3 - B_{22} Z_2 B_{12} I_1 \tag{1}$$

where Z_2 is the impedance matrix of RCL elements and $Z_l = B_{22} Z_2 B_{22}$. Equation (1) is called the *loop system of equations*.

- Step 2: Calculate I_2 using:

$$I_2 = B_{12} I_1 + B_{22} I_l \tag{2}$$

then,

$$V_2 = Z_2 I_2 \tag{3}$$

- Step 3: Determine V_1 and I_3 using the following:

$$V_1 = -B_{12} V_2 - B_{13} V_3 \tag{4}$$

$$I_3 = B_{13} I_1 + B_{23} I_l \tag{5}$$

Note that I_1 and V_3 have specified values, since they correspond to current and voltage sources, respectively.

B. Cutset Method of Network Analysis

- Step 1: Solve the following for the vector V_b (note that V_b is the vector of voltages in the nonsource branches of T):

$$Y_b V_b = -Q_{11} I_1 - Q_{12} Y_2 Q_{22} V_b \tag{6}$$

where Y_2 is the admittance matrix of RLC elements and $Y_b = Q_{12} Y_2 Q_{12}$. Equation (6) is called the *cutset system of equations*.

- Step 2: Calculate V_2 using:

$$V_2 = Q_{12} V_b + Q_{22} V_3 \tag{7}$$

then,

$$I_2 = Y_2 Y_2 \tag{8}$$

- Step 3: Determine V_1 and I_3 using the following:

$$V_1 = Q_{21} V_b + Q_{21} V_3 \tag{9}$$

$$I_3 = -Q_{21} I_1 - Q_{22} I_2 \tag{10}$$

Note that I_1 and V_3 have specified values, since they correspond to current and voltage sources.

This completes the cutset method of network analysis. Next we illustrate the loop and cutset methods of analysis on the network shown in Fig. 9. The graph of the network is shown Fig. 9b. We choose the spanning tree T consisting of edges 4, 5, and 6. Note that T contains the voltage source and has no current source. The fundamental circuit and the fundamental cutset matrices with respect to T are given below in the required partioned form:

$$B_f = \begin{array}{c c} & \begin{array}{cccccc} 1 & 2 & 3 & 4 & 5 & 6 \end{array} \\ & \begin{bmatrix} 1 & 0 & 0 & -1 & -1 & 1 \\ 1 & 1 & 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & 1 & -1 & 0 \end{bmatrix} \end{array}$$

$$Q_f = \begin{array}{c c} & \begin{array}{cccccc} 1 & 2 & 3 & 4 & 5 & 6 \end{array} \\ & \begin{bmatrix} 1 & -1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ -1 & 1 & 0 & 0 & 0 & 1 \end{bmatrix} \end{array}$$
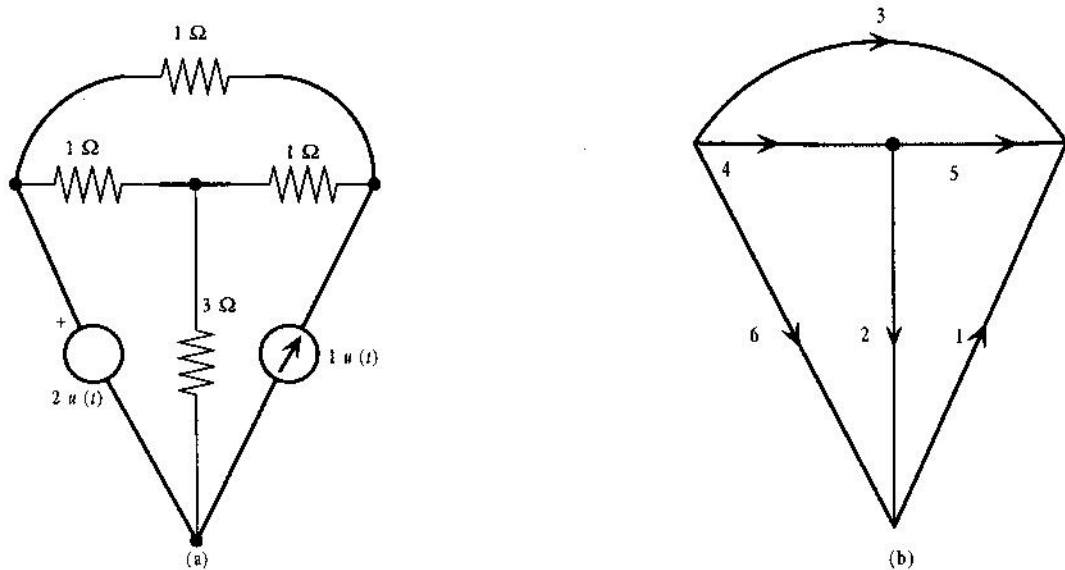
FIGURE 9 A network and its graph.

From these matrices we get:

$$B_{12} = \begin{bmatrix} 0 & 0 & -1 & -1 \end{bmatrix}$$

$$B_{13} = [1]$$

$$B_{22} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & -1 & -1 \end{bmatrix}$$

$$B_{23} = \begin{bmatrix} -1 \\ 0 \end{bmatrix}$$

$$Q_{11} = \begin{bmatrix} -1 \\ 0 \end{bmatrix}$$

$$Q_{12} = \begin{bmatrix} -1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}$$

$$Q_{21} = [-1]$$

$$Q_{22} = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix}$$

We also have

$$Z_2 = \begin{bmatrix} 3 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

$$Y_2 = \begin{bmatrix} 1/3 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

$$v_6 = 2 \text{ volts}$$

$$i_1 = 1 \text{ ampere}$$

C. Loop Method Example

Edges 2 and 3 are nonsource chords. So,

$$I_l = \begin{bmatrix} i_2 \\ i_3 \end{bmatrix}$$

Substituting

$$Z_l = B_{22} Z_2 B_{22}^t$$

$$= \begin{bmatrix} 4 & -1 \\ -1 & 3 \end{bmatrix}$$

in Eq. (1), we get the following loop system of equations:

$$\begin{bmatrix} 4 & -1 \\ -1 & 3 \end{bmatrix} \begin{bmatrix} i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} 3 \\ -2 \end{bmatrix}$$

Solving for i_2 and i_3, we get:

$$I_l = \begin{bmatrix} i_2 \\ i_3 \end{bmatrix} = 1/11 \begin{bmatrix} 7 \\ -5 \end{bmatrix}$$

Using Eq. (2), we get:

$$I_2 = \begin{bmatrix} i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = 1/11 \begin{bmatrix} 7 \\ -5 \\ 1 \\ -6 \end{bmatrix}$$

Then, using $V_2 = Z_2 I_2$, we get:

$$V_2 = \begin{bmatrix} v_2 \\ v_3 \\ v_4 \\ v_5 \end{bmatrix} = 1/11 \begin{bmatrix} 21 \\ -5 \\ 1 \\ -6 \end{bmatrix}$$

Finally, from Eqs. (4) and (5) we get:

$$V_1 = [v_1] = -27/11$$

$$I_3 = [i_6] = 4/11$$

D. Cutset Method Example

Edges 4 and 5 are the nonsource branches, so:

$$V_b = \begin{bmatrix} v_4 \\ v_5 \end{bmatrix}$$

Substituting

$$Y_b = \begin{bmatrix} 7/3 & 1 \\ 1 & 2 \end{bmatrix}$$

in Eq. (6), we get the following cutset system of equations:

$$Y_b V_b = \begin{bmatrix} 7/3 & 1 \\ 1 & 2 \end{bmatrix} \begin{bmatrix} v_4 \\ v_5 \end{bmatrix} = \begin{bmatrix} -1/3 \\ -1 \end{bmatrix}$$

Solving for V_b.

$$V_b = \begin{bmatrix} v_4 \\ v_5 \end{bmatrix} = 1/11 \begin{bmatrix} 1 \\ -6 \end{bmatrix}$$

From Eq. (7) we get:

$$V_2 = \begin{bmatrix} v_2 \\ v_3 \\ v_4 \\ v_5 \end{bmatrix} = 1/11 \begin{bmatrix} 21 \\ -5 \\ 1 \\ -6 \end{bmatrix}$$

Using

$$I_2 = Y_2 V_2$$

we get:

$$I_2 = \begin{bmatrix} i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = 1/11 \begin{bmatrix} 7 \\ -5 \\ 1 \\ -6 \end{bmatrix}$$

Finally, using Eqs. (9) and (10),

$$V_1 = [v_1] = -27/11$$

$$I_3 = [i_6] = 4/11$$

This completes our illustration of the loop and cutset methods of circuit analysis.

Suppose a network N has no independent voltage sources. Then a convenient description of N with the node voltages as independent variables can be obtained as follows. Let A be the incidence matrix of N with vertex v_r as reference. Let us also partition A as $A = [A_{11} \ A_{12}]$, where the columns of A_{11} and A_{12} correspond, respectively, to the RCL elements and current sources. If I_1 and I_2 denote the column vectors of RCL element currents and current source currents, then KCL equations for N become:

$$A_{11} = -A_{12} I_2$$

We also have

$$I_1 = Y_1 V_1$$

where V_1 is the column vector of voltages of RCL elements and Y_1 is the corresponding admittance matrix. Furthermore, by the node transformation we have:

$$V_1 = A_{11}^t V_n$$

where V_n is the column vector of node voltages. So, we get from the KCL equations:

$$(A_{11} Y_1 A_{11}^t) V_n = -A_{12} I_2$$

The above equations are called *node equations*. The matrix $A_{11} Y_1 A_{11}^t$ is called the *node admittance matrix* of N.

FURTHER READING

For a more comprehensive discussion of other developments in graph theoretic concepts, please consult Chen (1972, 2001), Swamy and Thulasiraman (1981), and Watanabe and Shinoda (1999). For a very good treatment of liner circuits and other releated references, see Balabanian and Bickart (1981). Mitra (1974) provides a very good early work on active networks, while Chua et al. (1987) and Hasler and Neirynck (1986) are good sources for nonlinear network theory.

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