- [10] R. Yarlagadda, "An application of tridiagonal matrices to network synthesis," SIAMJ. Appl. Math., Nov. 1968, pp. 1146-1162.
  [11] T. G. Marshall, "Synthesis of RLC ladder networks by tridiag-
- [11] T. G. Marshall, "Synthesis of RLC ladder networks by tridiagonalization," IEEE Trans. Circuit Theory, vol. CT-16, Feb. 1969, pp. 39-46.
  [12] T. R. Bashkow, "The A-matrix, new network description," IRE
- [12] T. R. Bashkow, "The A-matrix, new network description," IRE Trans. Circuit Theory, vol. CT-4, Sept. 1957, pp. 117-119.
- [13] A. Dervisoglu, "The realization of the A-matrix of a certain class of RLC networks," IEEE Trans. Circuit Theory, vol. CT-13, June 1966, pp. 164-170.
- [14] S. Seshu and M. B. Reed, Linear Graphs and Electrical Networks. Reading, Mass.: Addison-Wesley, 1961.
- [15] E. R. Fowler, "A unified state-space approach to RLCT two-port transfer function synthesis," Ph.D. dissertation, Oklahoma State Univ., Stillwater, May 1969.
- [16] S. Seshu and N. Balabanian, Linear Network Analysis. New York: Wiley, 1959.
- [17] F. Ye, "Network synthesis using nullators and norators," Ph.D. dissertation, Oklahoma State Univ., Stillwater, 1971.

# Synthesis of (*n* + 2)-Node Resistive *n*-Port Networks

#### P. SUBBARAMI REDDY AND K. THULASIRAMAN

Abstract—Certain properties of the network of departure  $N_d$  and the padding network  $N_p$  of an (n+2)-node resistive n-port network containing no negative conductances are established. Based on these properties, some necessary conditions and a sufficient condition for the realizability of the Y matrices of (n+2)-node resistive n-port networks are obtained. A new proof for the supremacy condition is given. Also, a necessary and sufficient condition for the realization of (n+2)-node n-port networks having specified Y and K matrices is given.

#### I. Introduction

THE PROBLEM of realization of a real symmetric matrix Y, as the short-circuit conductance matrix of a resistive *n*-port network having more than (n+1)nodes, has been a subject of research for more than a decade. Guillemin was the earliest to suggest a method of solution when the port configuration T of the required n-port network is specified [1]. His approach is based on the determination of 1) the unique network of departure  $N_d$  [5] with respect to the given matrix Y having the specified port configuration; and 2) a suitable padding n-port network  $N_p$  so that the parallel combination of  $N_d$  and  $N_p$  contains no negative conductances [5]. Later approaches [2]-[5] differ from Guillemin's only in the procedure used to generate padding n-port networks. The procedures given in [1], [2], and [5] to generate padding networks are general and applicable to the generation of all padding n-port networks having more than

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(n+1) nodes. The procedure given in [3] is applicable to (n+2)-node networks only and the one given in [4] can generate only a class of n-port networks whose potential factors are related in a special way. Frisch and Swaminathan [2] have also obtained a significant result, viz., the formulation of the supremacy condition, which is necessary for the realizability of the Y matrices of (n+2)-node n-port networks.

In this paper we consider the synthesis of (n+2)-node resistive *n*-port networks containing no negative conductances. Unless stated otherwise, we follow the notation used in [5]. In this section we restate certain results discussed in [5].

Consider an (n+2)-node resistive n-port network N containing no negative conductances. Permitting edges with zero conductances, the linear graph of N may be assumed to be complete. Let the two connected parts  $T_1$  and  $T_2$  of the port configuration T of N be linear trees. Let the vertices of any linear tree  $T_0$  of N, of which  $T_1$  and  $T_2$  are subgraphs, be numbered consecutively starting from one end vertex of  $T_0$ . Let the first (m+1) vertices be in  $T_1$  and the remaining vertices in  $T_2$ . Let the set of vertices of  $T_1(T_2)$  be denoted by  $V_1(V_2)$ . Let  $N_d$  and  $N_p$  denote the network of departure and the padding network of N, respectively. For all  $i \in V_1(V_2)$  and  $j \in V_2(V_1)$ , let  $S_i = \sum_i g_{ij}$ 

$$S_{i0} = \sum_{j} |(g_{ij})_d|$$
 for all j's for which  $(g_{ij})_d \leq 0$  (1)

and

$$S = \sum_{i \in V_1} S_i = \sum_{i \in V_2} S_i$$

$$S_0 = \sum_{i \in V_1} S_{i0} = \sum_{i \in V_2} S_{i0}. \tag{2}$$

The following expressions for the conductances of  $N_p$  have been obtained in [5].

$$(g_{ij})_p = \frac{-S_i S_j}{S}, \qquad i, j \in V_1(V_2)$$

$$(g_{ij})_p = \frac{S_i S_j}{S}, \qquad i \in V_1, \quad j \in V_2. \tag{3}$$

Denoting as in [5] the nonzero nonunity potential factors of N by  $k_1, k_2, \dots, k_n$ , let

$$P = [(1-k_1), (k_1-k_2), (k_2-k_3), \cdots, (k_{m-1}-k_m), k_m,$$

$$(1-k_{m+1}), (k_{m+1}-k_{m+2}), \cdots, (k_{n-1}-k_n), k_n].$$
 (4)

Let

$$R = P^{t}P = [r_{ij}]. \tag{5}$$

It has been shown in [5] that

$$(g_{ij})_p = -r_{ij}S, \quad i, j \in V_1(V_2)$$
 (6)

$$(q_{ii})_n = r_{ii}S, \qquad i \in V_1, \quad j \in V_2. \tag{7}$$

We note that (3), (6), and (7) have been obtained assuming that  $T_1$  and  $T_2$  are linear. Also, the  $(g_{ij})_p$  obtained by assuming arbitrary values for the  $S_i$  and  $r_{ij}$  define the padding network  $N_p$  of some *n*-port network N containing no negative conductances, provided the  $S_i$  are nonnegative and the  $k_i$  satisfy the conditions of [5, Theorem 3]. It follows from the results on padding networks obtained in [6] that (3), (6), and (7) can be used to generate (n+2) padding *n*-ports having any arbitrary connected port configurations. However, the synthesis of a matrix Y is a "cut-and-try" procedure because of the assumed values of the  $[r_{ij}]$ .

## II. NECESSARY CONDITIONS FOR THE REALIZATION OF Y MATRICES OF (n+2)-NODE n-PORT NETWORKS

In this section we establish certain properties of the network of departure  $N_d$  and the padding network  $N_p$  of a given (n+2)-node n-port network N containing no negative conductances. Some of these properties serve as necessary conditions for the realizability of the Y matrices of (n+2)-node n-port networks. We also give a simpler proof of the supremacy condition given in [2]. Proofs of some of the properties are not given here.

#### Property 1

- 1)  $(g_{ij})_p \ge 0$ , for all  $i \in V_1$ ,  $j \in V_2$ .
- 2)  $(g_{ij})_p \le 0$ , for all  $i, j \in V_1(V_2)$ .
- 3)  $(g_{ij})_d \ge 0$ , for all  $i, j \in V_1(V_2)$ .

#### Property 2

- 1) If  $(g_{ij})_d > 0$  for any  $i \in V_1$  and  $j \in V_2$ , then  $(g_{ij})_p > 0$ .
- 2) If  $S_{i0} > 0$ , then  $S_i > S_{i0}$ .

#### Property 3

For any pair of vertices i and  $j \in V_1(V_2)$ :

- 1) if  $(g_{ij})_d = 0$ , then either  $S_{i0} = 0$  or  $S_{i0} = 0$  or both;
- 2) if  $(g_{ij})_d = 0$  with  $S_{j0} \neq 0$ , then  $S_i = 0$ .

Let  $V_1^{\circ}$  be a subset of  $V_1$  such that for every  $i \in V_1^{\circ}$ ,  $S_{i0} = 0$ , and  $(g_{ij})_d = 0$  for some  $j \in V_1$ , with  $S_{j0} \neq 0$ . It is evident from Property 3-2) that for every  $i \in V_1^{\circ}$ ,  $S_i = 0$ .

Let the complement of  $V_1^{\circ}$  in  $V_1$  be denoted by  $V_1^{\circ}$ . Let  $V_1^{a}$  be a subset of  $V_1^{\circ}$  so that for every  $j \in V_1^{a}$ ,  $S_{j0} \neq 0$ , and there exists a  $k \in V_1^{a}$  such that

$$\frac{S_{j0}S_{k0}}{S_0} \ge (g_{jk})_d.$$

Since for all  $j \in V_1^a S_{j0} \neq 0$ , we have  $S_j > 0$  for all  $j \in V_1^a$ . Therefore, for all  $j, k \in V_1^a$ ,  $(g_{jk})_d > 0$ . Similarly,  $V_2^\circ$ ,  $V_2^a$ , and  $V_2^\circ$  are defined.

#### Property 4

For an (n+2)-node *n*-port network containing no negative conductances  $V_1^a \neq V_1^c$  and  $V_2^a \neq V_2^c$  (i.e.,  $V_1^a$  and  $V_2^a$  are proper subsets of  $V_1^c$  and  $V_2^c$ , respectively).

*Proof:* Let  $S_j = S_{j0} + x_j$ , where  $x_j \ge 0$  for all  $j = 1, 2, \dots, n+2$ , and let

$$\Delta = \sum_{j=1}^{m+1} x_j = \sum_{j=m+2}^{m+2} x_j.$$

For every  $j \in V_1^a$  there exists a  $k \in V_1^a$  so that

$$\frac{S_{j0}S_{k0}}{S_0} \geq (g_{jk})_d.$$

Since N contains no negative conductances,  $(g_{jk})_d \ge S_j S_k / S$ . Therefore,

$$\frac{S_j S_k}{S} \le \frac{S_j 0 S_{k0}}{S_0} .$$

i.e.,

$$\frac{(S_{j0} + x_j)(S_{k0} + x_k)}{S_0 + \Delta} \le \frac{S_{j0}S_{k0}}{S_0}$$

i.e.,

$$x_i x_k + S_{i0} x_k + S_{k0} x_i \le S_{k0} S_{i0} (\Delta / S_0).$$

Each term on the left-hand side of the above equation is positive, since for every  $j \in V_{1}^{a}$ ,  $x_{j} > 0$  [Property 2-2)]. Therefore.

$$\frac{S_{j0}S_{k0}\Delta}{S_0} > S_{k0}x_j$$
 and  $\frac{S_{j0}S_{k0}\Delta}{S_0} > S_{j0}x_k$ .

Therefore,

$$\frac{S_{j0}}{S_0} > \frac{x_j}{\Delta} \quad \text{and} \quad \frac{S_{k0}}{S_0} > \frac{x_k}{\Delta} .$$

Thus we have for all  $j \in V_1^a$ ,

$$\frac{S_{j0}}{S_0} > \frac{x_j}{\Delta} \tag{8}$$

Also, we have  $S_{j0} = S_j = 0$  for all  $j \in V_1^{\circ}$ . Therefore,

$$x_j = 0$$
, for every  $j \in V_1^{\circ}$ . (9)

Let (contrary to the theorem)

$$V_1^a = V_1^c$$

i.e.,

$$V_1^a \cup V_1^\circ = V_1$$
.

Then  $(S_{j0}/S_0)>(x_j/\Delta)$  if  $S_{j0}>0$  [from (8)], and  $x_j=0$  if  $S_{j0}=0$  [from (9)]. Hence it follows that

$$\sum_{j \in V_1} \frac{S_{j0}}{S_0} > \sum_{j \in V_1} \frac{x_j}{\Delta}, \quad \text{i.e., } 1 > 1.$$

Thus we observe that the assumption  $V_1^a = V_1^c$  leads to an absurdity. Therefore  $V_1^a \neq V_1^c$ ; similarly  $V_2^a \neq V_2^c$ . Hence the theorem.

In the following we shall refer to those (n+2)-node n-port networks for which  $y_{ij}=0$  for all  $i \in T_1$ ,  $j \in T_2$  as degenerate networks.

In nondegenerate networks, for every  $i \in V_1$  there exists a  $j \in V_1$ ,  $j \neq i$  so that  $S_{j0} \neq 0$ . For  $i \in V_1$ , let

$$m_{ij}^{(1)} = \frac{(g_{ij})_d}{S_{i0}}$$
, for all  $j \in V_1$  where  $S_{j0} \neq 0$ .

Let

$$M_{i^{(1)}} = \min \{m_{ij}^{(1)}\}$$

and

$$M^{(1)} = \sum_{i=1}^{m+1} M_i^{(1)}$$
.

Similarly,  $m_{ij}^{(2)}$ ,  $M_i^{(2)}$ , and  $M^{(2)}$  are defined. In a nondegenerate network, at least two  $M_i^{(1)}$  and at least two  $M_i^{(2)}$  are nonzero.

#### Property 5

For an (n+2)-node n-port network containing no negative conductances,  $M^{(1)} \ge 1$  and  $M^{(2)} \ge 1$ .

*Proof:* For any  $i, j \in V_1$ 

$$\frac{S_i S_j}{S} \le (g_{ij})_d.$$

Since  $S_i \ge S_{i0}$ , we have

$$\frac{S_i}{S} \leq \frac{(g_{ij})_d}{S_{j0}} = m_{ij}, \quad \text{for all } j \in V_1 \text{ for which } S_{j0} \neq 0.$$

. Since  $M_i^{(1)} = \min \{m_{ij}^{(1)}\}$ , it follows from the above that

$$M_i^{(1)} \geq \frac{S_i}{S}$$
.

We note that if  $M_i^{(1)} = 0$ , then  $S_i = 0$ . Thus we have

$$M^{(1)} = \sum_{i=1}^{m+1} M_i^{(1)} \ge \sum_{i=1}^{m+1} \frac{S_i}{S} = 1.$$

Therefore  $M^{(1)} \ge 1$ ; similarly,  $M^{(2)} \ge 1$ .

Property 6 (Supremacy Condition)

For an *n*-port network N containing no negative conductances, let there exist some vertices i and  $j \in V_1$  and some vertices k and  $l \in V_2$  so that

$$(g_{ik})_d \leq 0$$
 and  $(g_{jl})_d \leq 0$ .

Then

$$(g_{ij})_d(g_{kl})_d \geq |(g_{ik})_d| |(g_{jl})_d|.$$

Proof:

$$(g_{ij})_{p}(g_{kl})_{p} = \left(-\frac{S_{i}S_{j}}{S}\right)\left(-\frac{S_{k}S_{l}}{S}\right)$$

$$= \left(\frac{-S_{i}S_{k}}{S}\right)\left(\frac{-S_{j}S_{l}}{S}\right)$$

$$= (g_{ik})_{p}(g_{jl})_{p}.$$
(10)

Since N contains no negative conductances,

$$(g_{ij})_d \ge - (g_{ij})_p$$
  
 $(g_{kl})_d \ge - (g_{kl})_p.$  (11)

Also,

$$(g_{ik})_p \ge |(g_{ik})_d|$$

$$(g_{il})_p \ge |(g_{il})_d|.$$
(12)

Therefore, from (10)-(12), we get

$$(g_{ij})_d(g_{kl})_d \geq |(g_{ik})_d| |(g_{jl})_d|.$$

Of the properties discussed so far in this section some relate to the network of departure  $N_d$  and others relate to the padding n-port network  $N_p$  of a given (n+2)-node n-port network N. Since the network of departure  $N_d$  with respect to a given real symmetric matrix Y is unique and can be easily determined when the port configuration T is specified, the properties of  $N_d$  (Properties 3-6) can be used as necessary conditions for the realizability of Y matrices of (n+2)-node n-port networks.

## III. A SUFFICIENT CONDITION FOR THE REALIZATION OF Y MATRICES OF (n+2)-NODE RESISTIVE n-PORT NETWORKS

In this section we give a sufficient condition for the realization of a real symmetric matrix Y as the short-circuit conductance matrix of an (n+2)-node resistive n-port network having a 2-tree port configuration T.

Following the notation introduced in Section I, we define  $\sigma_1$  and  $\sigma_2$  as follows:

$$\sigma_1 = \min \left\{ \frac{(g_{ij})_d S_0}{S_{i0} S_{j0}} - 1 \right\}$$

for all  $i, j \in V_1$  or for all  $i, j \in V_2$  such that  $(g_{ij})_d > 0$ ,  $S_{i0} \neq 0$ ,  $S_{j0} \neq 0$ , and

$$\sigma_2 = \max \left\{ \frac{\left| (g_{ij})_d \right| S_0}{S_{i0} S_{i0}} - 1 \right\}$$
 (13)

for all  $i \in V_1$  and  $j \in V_2$  such that  $(g_{ij})_d < 0$ . We note that if  $(g_{ij})_d < 0$  for some  $i \in V_1$  and  $j \in V_2$ , then by (1),  $S_{i0} > 0$  and  $S_{j0} > 0$ . This ensures the existence of  $\sigma_2$ .

#### Theorem 1

A real symmetric matrix Y can be realized as the short-circuit conductance matrix of an (n+2)-node n-port network having a specified 2-tree port configuration T, if the following two conditions are met.

- 1) For all  $i, j \in V_1$  or for all  $i, j \in V_2$ :
  - a)  $(g_{ij})_d \ge 0$ ;
  - b)  $S_{i0}S_{j0}/S_0=0$ , if  $(g_{ij})_d=0$ ;
  - c) for some  $i, j \in V_1(V_2), S_{i0} > 0, S_{j0} > 0, \text{ and } (g_{ij})_d > 0$ ;
  - d)  $S_{i0}S_{j0}/S_0 < (g_{ij})_d$ , if  $(g_{ij})_d > 0$ .
- 2)  $\sigma_1 \geq \sigma_2$ .

It can be shown that the following steps will lead to a proper realization of a matrix Y satisfying the conditions of Theorem 1.

Step 1: Obtain the unique network of departure  $N_d$  with respect to Y and having the specified port configuration T.

Step 2: Choose  $\Delta$  so that  $S_0\sigma_2 \leq \Delta \leq \sigma_1 S_0$ .

Step 3: Obtain  $S_i$  so that  $S_i = S_{i0}(1 + \Delta/S_0)$ .

Step 4: Obtain a padding n-port network  $N_p$  so that

$$(g_{ij})_p = -\frac{S_i S_j}{S}$$
, for all  $i, j \in V_1$  or  $i, j \in V_2$ ,  $j \neq i$   
 $(g_{ij})_p = \frac{S_i S_j}{S}$ , for all  $i \in V_1$  and  $j \in V_2$ .

Step 5: The parallel combination of  $N_d$  and  $N_p$  will represent a proper realization N of the given Y.

It is interesting to note that all *n*-port networks obtained using different values of  $\Delta$  will have the same modified cut-set matrix [5]. This follows from the fact that

$$k_i = \sum_{j=i+1}^{m+1} \frac{S_j}{S} = \sum_{j=i+1}^{m+1} \frac{S_{j0}}{S_0}, \quad i \leq m$$

OF

$$k_i = \sum_{j=i+2}^{n+2} \frac{S_j}{S} = \sum_{j=i+2}^{n+2} \frac{S_{j0}}{S_0}, \quad i \ge m+1.$$

We observe that the sufficient condition stated in Theorem 1 is also necessary and sufficient for 2-port networks with 4 terminals.

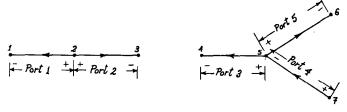


Fig. 1. Port configuration used in Example 1.

#### Example 1

Let it be required to realize the matrix Y given by

$$Y = \begin{bmatrix} 32 & -32 & -4 & 20 & 2 \\ -32 & 80 & 4 & -20 & -2 \\ -4 & 4 & 25 & 7 & -3 \\ 20 & -20 & 7 & 38 & 7 \\ 2 & -2 & -3 & 7 & 13 \end{bmatrix}$$

as the short-circuit conductance matrix of a resistive 5-port network having the port configuration shown in Fig. 1.

The conductances of the network of departure  $N_d$  with respect to Y and having the prescribed port configuration are given by

$$G_d = \operatorname{diag} \left\{ g_{12} \quad g_{13} \quad g_{14} \quad g_{15} \quad g_{16} \quad g_{17} \quad g_{23} \quad g_{24} \quad g_{25} \quad g_{26}$$

$$g_{27} \quad g_{34} \quad g_{35} \quad g_{36} \quad g_{37} \quad g_{45} \quad g_{46} \quad g_{47} \quad g_{56} \quad g_{57} \quad g_{67} \right\} d$$

$$= \operatorname{diag} \left\{ 0 \quad 32 \quad 4 \quad -22 \quad -2 \quad 20 \quad 48 \quad 0 \quad 0 \quad 0 \quad 0 \right.$$

$$\left. -4 \quad 22 \quad 2 \quad -20 \quad 15 \quad 3 \quad 7 \quad 3 \quad 24 \quad 7 \right\}.$$

We observe that  $S_0 = 48$ . We obtain  $\sigma_1$  and  $\sigma_2$  as  $\sigma_1 = 89/55$ ,  $\sigma_2 = 1$ . We must choose a value of  $\Delta$  in the range  $48 \le \Delta \le 89/55 \times 48$ . Choosing  $\Delta = 48$ , we get the  $S_1$  as

$$S_1 = 48$$
  $S_2 = 0$   $S_3 = 48$   $S_4 = 8$   
 $S_5 = 44$   $S_6 = 4$   $S_7 = 40$   $S = 96$ 

The conductances of the required padding network  $N_p$  having the above values of the  $S_i$  are given by

$$G_p = \text{diag} \left\{ 0 -24 \ 4 \ 22 \ 2 \ 20 \ 0 \ 0 \ 0 \ 0 \ 4 \ 22 \ 2 \right.$$
  
 $20 -11/3 -1/3 -10/3 -11/6 -110/6 -5/3 \right\}.$ 

The parallel combination of  $N_d$  and  $N_p$  is a 5-port network realizing the given Y matrix.

#### IV. Synthesis of (n+2)-Node Resistive n-Port Networks Having Prescribed Yand K Matrices

Given a real symmetric matrix

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$$

with  $Y_{11}$  and  $Y_{22}$  uniformly tapered and a K matrix [5] equal

to

$$\begin{bmatrix} \longleftarrow m \longrightarrow \longleftarrow n - m \longrightarrow \\ K_{11} & K_{12} \\ K_{21} & K_{22} \end{bmatrix} n \xrightarrow{\uparrow} m$$

with  $K_{11}$  and  $K_{22}$  having the forms

we obtain in this section a necessary and sufficient condition for the synthesis of an (n+2)-node resistive n-port network containing no negative conductances and having Y and K as its short-circuit conductance and potential factor matrices, respectively, and a linear 2-tree port configuration T, the connected parts  $T_1$  and  $T_2$  of T being defined by  $K_{11}$  and  $K_{22}$ , respectively. Also,  $Y_{11}$  and  $Y_{22}$  correspond to  $K_{11}$  and  $K_{22}$ , respectively.

Following the notation introduced in Section I, let

$$L_1 = \min \left\{ \frac{(g_{ij})_d}{r_{ij}} \right\} \tag{14}$$

for all  $i, j \in V_1$  or for all  $i, j \in V_2, j \neq i$ , provided  $(g_{ij})_d > 0$  and  $r_{ij} > 0$  and

$$L_2 = \max \left\{ \frac{\left| (g_{ij})_d \right|}{r_{ii}} \right\} \tag{15}$$

for all  $i \in V_1$  and  $j \in V_2$ , provided  $(g_{ij})_d < 0$ .

#### Theorem 2

A necessary and sufficient condition for the synthesis of an (n+2)-node resistive *n*-port network N containing no negative conductances and having a linear 2-tree port configuration and Y and K as its short-circuit conductance and potential factor matrices, respectively, is the following:

$$k_{i,1} = k_{i,2} = \cdots = k_{i,m} = k_i, \quad \text{if } i \ge m+1$$

$$k_{i,m+1} = k_{i,m+2} = \cdots = k_{i,n} = k_i, \quad \text{if } i \le m.$$

$$1 > k_1 \ge k_2 \ge \cdots \ge k_m$$

$$1 > k_{m+1} \ge k_{m+2} \ge \cdots \ge k_n.$$

- 1) If for any  $i, j \in V_1(V_2), (g_{ij})_d = 0$ , then  $r_{ij} = 0$ .
- 2)  $(g_{ij})_a \ge 0$  for all  $i, j \in V_1(V_2)$  and there exists at least one pair of vertices  $i, j \in V_1(V_2)$  such that  $(g_{ij})_a > 0$  and  $(r_{ij}) > 0$ .
  - 3) if  $(g_{ij})_d < 0$  for any  $i \in V_1$  and  $j \in V_2$ , then  $r_{ij} > 0$ .

$$L_1 \geq L_2$$
.

It can be shown that the following procedure will lead to an (n+2)-node n-port network containing no negative conductances if the conditions of Theorem 2 are satisfied.

Fig. 2. Port configuration used in Example 2.

Step 1: Obtain the unique network of departure  $N_d$  with respect to the given matrix Y and having the prescribed port configuration.

Step 2: Calculate the  $r_{ij}$  and  $L_1$  and  $L_2$ .

Step 3: Choose an S in the interval  $L_2 \leq S \leq L_1$ .

Step 4: Use the value of S obtained in Step 3 to obtain an  $N_p$  whose conductances are obtained, using (6) and (7).

Step 5: The parallel combination N of  $N_p$  and  $N_d$  will contain no negative conductances and will be a realization of Y and K.

#### Example 2

Let it be required to synthesize a 4-port resistive network having the matrices Y and K as its short-circuit conductance and potential factor matrices, respectively:

$$Y = \begin{bmatrix} 67 & 45 & -6 & 2 \\ 45 & 62 & 5 & 15 \\ -6 & 5 & 60 & 40 \\ 2 & 15 & 40 & 55 \end{bmatrix}$$

$$K = \begin{bmatrix} 1 & 1 & 0.6 & 0.6 \\ 0 & 1 & 0.5 & 0.5 \\ 0.4 & 0.4 & 1 & 1 \\ 0.3 & 0.3 & 0 & 1 \end{bmatrix}.$$

Following the procedure given in [7], it can be shown that the port configuration corresponding to the given K matrix will be as shown in Fig. 2.

We note that  $k_1 = 0.6$ ,  $k_2 = 0.5$ ,  $k_3 = 0.4$ , and  $k_4 = 0.3$ . The conductances of the required network of departure  $N_d$  are obtained as

$$G_{d} = \operatorname{diag} \left\{ g_{12} \quad g_{13} \quad g_{14} \quad g_{16} \quad g_{16} \quad g_{23} \quad g_{24} \quad g_{25} \quad g_{26} \quad g_{34}$$

$$= \operatorname{diag} \left\{ 22 \quad 45 \quad 6 \quad -8 \quad 2 \quad 17 \quad -11 \quad -2 \quad 13 \quad 5 \right.$$

$$= 10 \quad -15 \quad 20 \quad 40 \quad 15 \right\}.$$

We obtain  $R = [r_{ij}]$  as follows:

$$R = \begin{bmatrix} 0.16 & 0.04 & 0.2 & 0.24 & 0.04 & 0.12 \\ 0.04 & 0.01 & 0.05 & 0.06 & 0.01 & 0.03 \\ 0.2 & 0.05 & 0.25 & 0.3 & 0.05 & 0.15 \\ 0.24 & 0.06 & 0.3 & 0.36 & 0.06 & 0.18 \\ 0.04 & 0.01 & 0.05 & 0.06 & 0.01 & 0.03 \\ 0.12 & 0.03 & 0.15 & 0.18 & 0.03 & 0.09 \end{bmatrix}$$

We next obtain  $L_1$  and  $L_2$ , as  $L_1 = 2000/9$  and  $L_2 = 200$ . We must choose a value of S in the range  $200 \le S \le 2000/9$ . Choosing S = 200, and using (6) and (7), the conductances of

the required padding network  $N_p$  are obtained as

$$G_p = \text{diag} \left\{ -8 -40 \ 48 \ 8 \ 24 -10 \ 12 \ 2 \ 6 \ 60 \right\}$$

The parallel combination of  $N_p$  and  $N_d$  realizes the matrices Y and K.

#### V. CONCLUSIONS

The approach adopted by Guillemin [1] toward the n-port synthesis problem suggests that a greater insight into the nature of the problem can be obtained from a study of the networks of departure and padding networks of resistive n-port networks containing no negative conductances. The conductances of the networks of departure being linear functions of the elements of the Y matrix, it is possible to establish from the properties of these networks conditions for the realizability of Y matrices of n-port networks. Frisch and Swaminathan 2 were the first to work in this direction and they formulated the supremacy condition. The necessary conditions and the sufficient condition obtained in this paper for the realization of Y matrices of (n+2)-node resistive n-port networks further underline the importance and usefulness of Guillemin's approach to the *n*-port synthesis problem.

Whereas synthesis of n-port networks having specified Y matrices involves solution of nonlinear equations, synthesis of networks having specified Y and also K matrices is, as

shown in [6], straightforward requiring the solution of linear programs. Theorem 2 of this paper provides a simple solution of the latter problem for the special case of (n+2)-node n-port networks.

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#### REFERENCES

- [1] E. A. Guillemin, "On the realization of an nth-order G matrix," *IEEE Trans. Circuit Theory*, vol. CT-8, Sept. 1961, pp. 318-323.
- [2] K. R. Swaminathan and I. T. Frisch, "Necessary conditions for the realizability of *n*-port resistive networks with more than (*n*+1) nodes," *IEEE Trans. Circuit Theory*, vol. CT-12, Dec. 1965, pp. 520-527
- [3] F. J. Lupo and C. C. Halkias, "Synthesis of *n*-port networks on two-tree port-structures," *IEEE Trans. Circuit Theory*, vol. CT-12, Dec. 1965, pp. 571–577.
- [4] F. J. Lupo, "The synthesis of transformerless *n*-port networks on multitree port structures," *IEEE Trans. Circuit Theory*, vol. CT-15, Sept. 1968, pp. 211–220.
- [5] P. Subbarami Reddy, V. G. K. Murti, and K. Thulasiraman, "Realization of modified cut-set matrix and applications," *IEEE Trans. Circuit Theory*, vol. CT-17, Nov. 1970, pp. 475-486.
- [6] P. Subbarami Reddy and K. Thulasiraman, "Synthesis of the K-matrix of n-port networks and applications," presented at the 1970 IEEE Int. Symp. Circuit Theory, Atlanta, Ga.
- IEEE Int. Symp. Circuit Theory, Atlanta, Ga.

  [7] A. Lempel and I. Cederbaum, "The K matrix of n-port networks: Analysis and synthesis," IEEE Trans. Circuit Theory, vol. CT-16, Nov. 1969, pp. 471–483.

### Some New Configurations for Active Filters

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Abstract—Some new active-filter configurations based on the pole—zero cancellation technique are introduced. First, for the range Q  $\leq$  50 a single-amplifier circuit is suggested. For higher selectivity (50 < Q  $\leq$  500) a two-amplifier circuit is proposed. Another easily cascadable two-amplifier circuit with a reduced number of capacitors is discussed. In the latter case the

filter function is determined by certain resistive ratios. All the configurations proposed employ integrated circuit operational amplifiers (OAs). The sensitivity problem is discussed in detail. Effects of the finite OA frequency response are also investigated.

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#### I. Introduction

O DATE all general active-filter synthesis methods, with a few notable exceptions, have the drawback of increasing element sensitivities as the Q of the transfer-function poles and zeros increase. This fact is primarily due to the dependence upon differences of polynomials to synthesize denominators and/or numerators of the required transfer function [1]-[3]. In fact, it has been shown that some