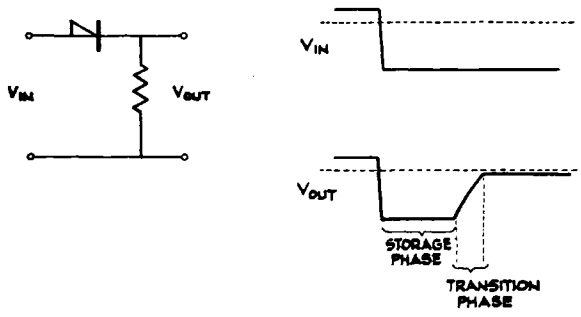

Fig. 1. Single-diode pulse generator.

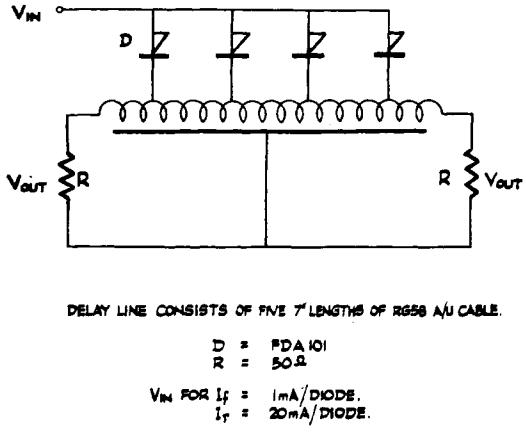

Fig. 2. 1-GHz 4-diode pulse generator.

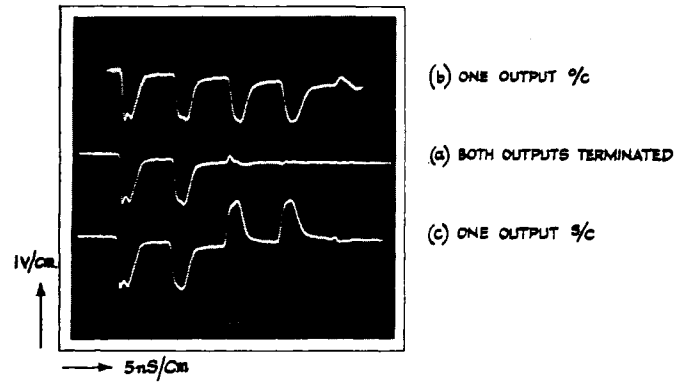

Fig. 3. 100-MHz bit rate 2-diode generator.

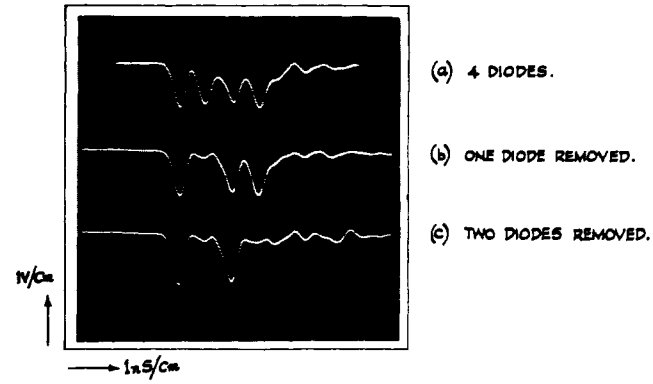

Fig. 4. 1-GHz bit rate 4-diode generator.

Provided the pulse width is less than the delay between tapping points, and the reverse biased diode capacitance does not introduce discontinuities on the delay line, a series of pulses will propagate in each direction down the line. Such a pulse generator with a number of equally spaced tapping points could be used to generate digital words by the omission of selected diodes along the line.

The pulse characteristics are dependent upon the same factors that influence the generation of single pulses, and upon any degradation of the pulse which may take place during transmission down the line. Thus the pulse width is dependent upon carrier lifetime, stored charge, and the rate of recovery of charge, and the rise and fall times upon the rise time of the input pulse and the diode characteristics. The word repetition rate is the same as the input pulse rate.

Many variations on the basic idea are possible, including the selective omission of diodes to produce words, the use of diodes of different characteristics or similar diodes with differing forward currents to produce more complex waveforms, and the application of transmission line discontinuities to produce reflected pulses. The basic generator produces two words propagating in opposite directions down the line with time inverted bit order. One method of combining these two words uses the reflecting properties of a mismatched transmission line; an open circuit at one output will enable both words to be extracted at the other output. Alternatively, termination of the line by a short circuit will give reflected bits of inverted polarity.

The method is particularly suited to the generation of words with high bit rates, and using currently available diodes the effective bit rate is in excess of 1 GHz. The effect of various line terminations upon the output produced by a 100-MHz 2-diode pulse generator is shown in Fig. 3. Waveforms for the 1-GHz pulse generator of Fig. 2 are shown in Fig. 4 and illustrate the effect of removing diodes from the line.

The system has advantages of cheapness, ease of construction, and the generation of complex waveforms at extremely high bit rates. It has applications in checking high-speed digital circuitry, particularly the response and resolution of high-speed nuclear counters. There is a possible use as a parallel-to-serial convertor if the forward current of the diode is controlled by the parallel information. Disadvantages include the high temperature coefficient of stored charge with its attendant effect on pulse width and the dc shift of the base line at the output by the forward current of the diodes. Excessive shift of the base line can be prevented by strapping very fast, low stored charge diodes to earth at one or more of the tapping points.

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Parallel Connection of n-Port Networks

***Abstract*—The conditions under which the parallel combination of two n-port networks has a short-circuit admittance matrix which is equal to the sum of the short-circuit admittance matrices of the component networks are examined. A convenient test involving the modified cut-set matrix of each network is presented.**

Consider two n-port networks N_1 and N_2 with Y_1 and Y_2 as their short-circuit admittance matrices. Let the terminal pair (i, i') constitute the ith port in each network with terminal i having the positive reference polarity. We ask the familiar question: Under what conditions does the combined network with N_1 and N_2 connected in parallel have a short-circuit admittance matrix equal to $(Y_1 + Y_2)$? A straightforward extension of the well-known test procedure applicable to 2-port networks leads to the following analysis.

Let, in the network N_1, $K_{ij}V$ be the potential of the terminal j with respect to the terminal i', when the ith port is connected to a voltage source V and all the other $(n-1)$ ports are short-circuited. K_{ij} may be termed the

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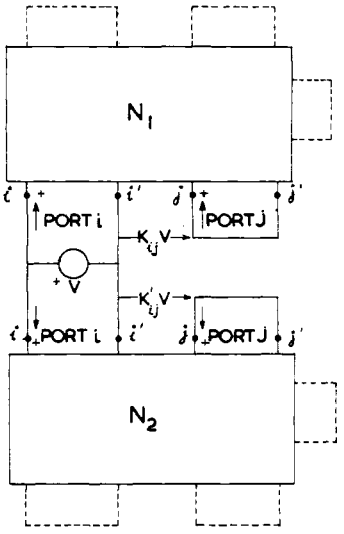

Fig. 1. Definition of potential factors.

potential factor of the jth port with respect to the ith port.[1] Similarly K'_{ij} for the network N_2 (see Fig. 1). In general, the potential factors are functions of the complex frequency variable s. If no circulating currents are to arise from the parallel connection of N_2 with N_1, we require that $K_{ij}=K'_{ij}$ for every i and j. In answer to the above question we then have the criterion: "If $[K_{ij}]$ and $[K'_{ij}]$, the matrices of the potential factors of the two networks, are equal, then the parallel combination of N_1 and N_2 has a resultant Y matrix equal to the sum of the Y matrices of the component networks." Application of this or any other equivalent test requires all the potential factors to be separately evaluated. To this end, if we employ the node-pair method of analysis, it involves the inversion of a $(v-n-1)$ by $(v-n-1)$ order matrix for each row of $[K_{ij}]$, where v is the number of vertices in N_1, and a similar amount of computation for $[K'_{ij}]$.

We now proceed to give an alternate criterion in terms of the modified cut-set matrix introduced by Cederbaum.[2] We consider networks N_1 and N_2 each having the same number of vertices v and no internal vertices; i.e., each of the vertices present forms a terminal of one or more ports. Evidently, $(n+1)\leq v\leq 2n$. Further, the graph of each network is taken to be complete and zero values of edge admittances permitted. Each edge is designated by the pair of vertices it joins, e.g., e_{pq} is the edge joining vertices p and q.

Now consider the fundamental cut-set matrix $[C_1/C_2]$ of the graph of the network N_1 with respect to a tree which includes the edges shunting the ports. Let C_1 correspond to these edges and C_2 to the remaining $(v-n-1)$ branches of the tree. Using the subscript b to denote the voltages of the latter set, the subscript p for port voltages and currents, and the subscript e for general edge voltages and admittances, we have

$$\begin{bmatrix} I_p \\ \hline 0 \end{bmatrix} = \begin{bmatrix} C_1 \\ \hline C_2 \end{bmatrix} [Y_e] [C'_1\ C'_2] \begin{bmatrix} V_p \\ \hline V_b \end{bmatrix}, \tag{1}$$

which on simplification leads to

$$[I_p] = [CY_eC'][V_p], \tag{2}$$

where

$$C = C_1 - [C_1Y_eC'_2][C_2Y_eC'_2]^{-1}[C_2]. \tag{3}$$

C is termed the modified cut-set matrix and we have the following relations:

$$Y_1 = CY_eC' \tag{4}$$

and

$$V_e = C'V_p. \tag{5}$$

Theorem 1: The element of the matrix C in the ith row and the column corresponding to the edge e_{pq} is equal to the voltage that appears across the edge e_{pq} when port i is excited with a source of unit voltage and all the other ports are short-circuited.

Theorem 2: Each element of C is a linear combination of the potential factors K_{ij}. Further, for every K_{ij} there exist two elements of C equal to it.

Theorem 1 follows directly from (5). When the ith port is excited with a unit-voltage source and all the other ports are short-circuited, the voltages across all the branches of the chosen tree are expressible as linear algebraic functions of the potential factors. It then follows that the voltages across all edges can be expressed likewise. This in conjunction with Theorem 1 proves the first part of Theorem 2. Since we have assumed a complete graph in setting up C and since every K_{ij} is the potential across two edges, $e_{i'j}$ and $e_{i'j'}$ under appropriate conditions, the second part of Theorem 2 follows.

It is thus seen that if the networks N_1 and N_2 are to have identical potential factors, their modified cut-set matrices must be equal. This leads to the following new criterion.

Theorem 3: The short-circuit admittance matrix Y of the parallel combination of two n-port networks with no internal vertices and having identical edge and port orientations is given by the sum of the short-circuit admittance matrices of the component networks, provided their modified cut-set matrices with identical row and column ordering are equal.

The application of the test in Theorem 3 requires for each network the calculation of the inverse of only one $(v-n-1)$ by $(v-n-1)$ matrix in contrast to the direct method where n such matrices are to be inverted. Further, once a given pair of networks N_1 and N_2 comply with the requirement contained in Theorem 3, the individual Y's or the combined Y can be directly evaluated using equations of the type in (4) and recognizing that the combined network retains the same C for its modified cut-set matrix.

The method given above can be readily extended to networks containing internal vertices. This and other matters relating to the form and properties of the modified cut-set matrix C will be covered in a future paper.

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A Dual Offset Gate Thin-Film Transistor

***Abstract*—A four-terminal thin-film transistor which provides voltage amplification with variable transconductance and threshold is described. The device structure incorporates the novel feature of asymmetric insulated gates on the opposite faces of a polycrystalline cadmium selenide film. Experimental data describing the device operation are presented.**

An experimental four-terminal thin-film transistor has been constructed which provides voltage amplification with variable transconductance and threshold. The structure, produced entirely by vacuum deposition through stencil masks, incorporates the novel feature of asymmetric dual gates. As shown in Fig. 1, the insulated gates are placed on opposite faces of the semiconductor film, with one gate offset toward the source, the other toward the drain.

Double gate transistors of the junction gate type are commercially available and several models of their operation have been analyzed [1]–[5]. Dual gate MOS devices have also been reported [6], [7]. Abraham and Poehler [8] described a TFT with two gates in a symmetrical "over and under" configuration in their work on field ionization of donors. Using silicon-on-sapphire heteroepitaxial techniques, Zuleeg and Knoll [9] fabricated a thin-film space-charge-limited triode incorporating a single gate offset toward the source.

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