The FFT has clear advantages over the matrix-vector product approach when a traditional model of computational complexity is used. In VLSI technology, though, where communication costs are more visible, the FFT's virtues merit a new scrutiny. Its throughput is not asymptotically higher and its area is not asymptotically smaller than the matrix-vector product design. In sum, if it retains computational complexity advantages, they would seem not to be asymptotic.

V. Conclusion

The use of "free accumulation" leads to simple, regular inner-product designs. We have given some details of an FIR filter and a linear transform design.

Convolution (polynomial product) is another computation that benefits from this approach. In the case of polynomial product, the word-level structure and algorithm are nearly perfectly analogous to the bit-level structure and algorithm (for integer product). There is no analog in polynomial product to the carries of integer product. This incongruity is slight; the topology of the two designs is the same: a hex-connected array.

Perhaps most intriguing is the fate of the FFT in a VLSI environment. In DFT applications where there is

1) no short latency requirement,
2) a high throughput requirement,
3) need for either only a portion of transformed components, or nonuniform sampling of the transformed domain,

the linear transform architecture presented in this paper may be more suitable than the an FFT architecture.

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On Description and Realization of Resistance n-Port Networks

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Abstract—**Remarks and results recently published in [1] are discussed.**

I. Introduction

In a recent note Betrand [1] has made certain remarks and a conjecture relating to the resistance n-port network problem. In this paper we comment on his remarks and the conjecture and point out an error in one of his results. We also draw attention to several other published results which are of interest in this connection.

II. Properties of the K-Matrix

First, Betrand establishes a few properties (property 1, and corollaries 1–3) relating to the K-matrix of $(n+1)$-node networks. In this context, we would like to point out that these properties have been referred to earlier in [2]–[6]. Furthermore, a simple algorithmic solution to the problem of synthesizing the K-matrix of $(n+1)$-node networks was reported in [5]. This algorithm is based on the above-mentioned properties as well as a few others also described in [5].

Secondly, the statement of property 2 of [1] is incorrect. The proof of this property is based on the following argument:

> "However, $x_{1j} = \hat{x}_{ij}$, $(j = 2, \cdots, k)$ because the only difference between the two configurations of Figs. 1 and 2 is the admittance across the nodes to which part 1 has been reduced."

There is an obvious error in this argument. The author has clearly overlooked the fact that there are admittances connecting nodes a and b in part 1 of Fig. 1 to the nodes in the remaining parts. Similarly there are admittances connecting nodes c and d in part 1 of Fig. 2 to the nodes in the remaining parts. As a result, the networks in Figs. 1 and 2 are distinctly different. So, $x_{1j} \neq \hat{x}_{ij}$, $(j = 2, \cdots, k)$.

The correct statement of property 2 is given below:

Property: If a purely resistive network is realized by a topological structure that has $(n + k)$ nodes $(1 \leqslant k \leqslant n)$, the elements of the K-matrix can be expressed in terms of $n(k-1)$ parameters. □

Proof of this property is easy if we note that in each row of the K-matrix there are $(k-1)$ distinct elements which are not zero or one. These $(k-1)$ elements correspond to the $(k-1)$ parts each of which is reduced to a single node, when the port under consideration is excited with a 1-V source and all the other ports are short-circuited. This property also has been referred to in several papers [3],[4],[6]–[8].

Consider next the (3×3)-matrix used in the example. This matrix is the K-matrix of a 3-port network whose port structure is in two disconnected parts. As stated in the above property, this K-matrix has three distinct elements which are neither zero nor one. These elements are: $k_{12}, k_{32}, k_{21} = k_{23}$. Thus the describing equations involve three variables and not *two* as remarked in [1]. Furthermore, the product "$k(k-1)$" occurring in the last paragraph of [1] should be changed to "$n(k-1)$."

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III. Realization of K and Y Matrices

An n-port network on $(n+k)$ nodes has $N_e=(n+k)(n+k-1)/2$ edge admittances. The corresponding Y-matrix has $N_y=n(n+1)/2$ distinct elements. Clearly $N_e \geq N_y$.

In the case of an $(n+1)$-node network, $N_e=N_y$. Thus in this case, there are as many Y-matrix elements as the number of edge admittances. Furthermore, the equations relating the Y-matrix elements and the edge admittances are linear. To obtain these equations, the port graph corresponding to the Y-matrix should be determined, and it can be easily determined [9],[10]. Thus an algorithmic solution is possible when $k=1$.

Suppose $k>1$. Then $N_e>N_y$. So in this case any procedure to synthesize an $(n+k)$-node n-port network from a given Y-matrix would involve $N_e-N_y=n(k-1)+k(k-1)/2$ parameters. Furthermore, the equations relating the Y-matrix elements and the edge admittances are nonlinear. So, to obtain an algorithmic synthesis procedure, additional information besides the Y-matrix is required. The specification of the K-matrix (along with the Y-matrix) has been helpful. The K-matrix, while uniquely determining the port graph, also gives values of $n(k-1)$ parameters as stated in the above property. Furthermore, the equations relating the Y-matrix and K-matrix elements to the edge admittances are linear. So, in the case of $(n+k)$-node n-port networks, the synthesis would involve determining $k(k-1)/2$ parameters satisfying certain linear inequalities if both the Y and K matrices are specified. This is how the synthesis procedure given in [3],[4] proceeds. In these papers it was shown that the problem of synthesizing an $(n+k)$-node n-port resistance network having specified Y and K matrices is only as complex as the problem of solving a linear program involving $k(k-1)/2$ variables which are related in a simple fashion to the edge admittances of the final realization. Thus *an algorithmic synthesis procedure is possible when both the Y and K matrices are specified.* So it is not clear why in the introductory section of [1] Betrand states that the K and Y matrix characterization "does not lead to an algorithmic synthesis procedure."

Finally, we comment on Betrand's conjecture.

Algorithmic synthesis procedures are available to synthesize a 3-port resistance network having a specified Y-matrix. For a discussion of these procedures, [11] and [12] may be referred. In this context, Betrand observes that in the case of 3-port networks both the Y-matrix and the K-matrix have the same number of independent elements. According to his conjecture, it is this fact that has made possible the algorithmic synthesis procedure (from a specified Y-matrix) in the case of 3-port networks. We do not agree with this for the following reasons.

The procedures in [11] and [12] both assume a port graph in two disconnected parts. Hence $N_e-N_y=4$ parameters are involved. Both these procedures set four edge admittances (of the final realization) to zero and thus obtain the information required to determine the values of the four parameters uniquely. Of course, the set of four edge admittances to be set to zero in the final realization cannot be chosen arbitrarily. On the other hand, the procedure described in [13] sets an appropriately selected set of three edge admittances to zero and obtains a number of continuously equivalent realizations by varying the value of the only parameter in a continuous range. Note that in the case of a 3-port network, $N_e=10$ when $k=2$, and that selecting an appropriate set of four edge admittances to be set to zero is not difficult because a number of the $\binom{10}{4}$ possibilities can be disregarded using considerations such as connectivity. Thus *algorithmic synthesis procedures have become possible in the 3-port case because of the ease with which additional information to fix the four parameters could be obtained.* Furthermore, if $n=3$ and $k=3$, then $N_e=15$ and the number of parameters is nine. Selecting an appropriate set of 9 parameters involves searching through a space of $\binom{15}{9}$ possibilities, and it is not easy. Perhaps this is the reason why no general algorithmic synthesis procedure has yet been attempted with $k=3$.

The complexity of the synthesis problem from a specified Y-matrix when $n>3$ is easy to see from the above. It involves searching a space of $\binom{N_e}{N_e-N_y}$ possibilities and indeed such a search would require exponential time. Furthermore only those possibilities which lead to linear inequalities as in the case of simultaneous realization of K and Y matrices will be useful. One way to reduce the search space is to identify those edge admittances which cannot assume zero value in the final realization. With this in view, a lower bound is given in [4] on the total number of nonzero edge admittances in any network realizing a given Y-matrix and having a specified port graph. Certain other results in this direction (for example, the supremacy condition) were reported in [14],[15].

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