Theorem 2: A necessary condition for the coefficients of the VTF of an LPS,

$$T_v = \frac{\sum_0^n a_i s^i}{\sum_0^m b_i s^i} \quad \text{is} \quad \frac{b_i}{a_i} \le \frac{b_{i+1}}{a_{i+1}}$$

the equality sign holding only when $i > n$.

Proof: $K_{\max}$ for LP is that required to adjust the Bode plot such that its maximum is 0 dB. For LPS, this always occurs at $w=0$. Therefore, $K_{\max} = b_0/a_0$. The Fialkow–Gerst conditions require $a_i \le b_i$ and hence

$$K_{\max} = \frac{b_0}{a_0} \le \text{minimum of} \frac{b_i}{a_i}, \qquad i = 1, 2, \cdots, n.$$

From Theorem 1, we have

$$K_{\max} \text{ of } T_{v_{\text{PD}}}{}^{(1)} = \frac{b_1}{a_1} \le \text{minimum of} \frac{b_i}{a_i}, \qquad i = 2, \cdots, n.$$

Hence, it follows that

$$\frac{b_0}{a_0} \le \frac{b_1}{a_1} \le \frac{b_i}{a_i}, \qquad i = 2, 3, \cdots, n.$$

A continuation of the argument gives

$$\frac{b_0}{a_0} \le \frac{b_1}{a_1} \le \frac{b_2}{a_2} \le \cdots \le \frac{b_n}{a_n}$$

which can be written as

$$\frac{b_i}{a_i} \le \frac{b_{i+1}}{a_{i+1}}, \qquad i = 0, 1, \cdots, n+1.$$

Consider the equality sign. Let $b_0/a_0 = b_1/a_1$, from which we have

$$\frac{b_0/b_m}{a_0/a_n} = \frac{b_1/b_m}{a_1/a_n}. \tag{2}$$

But

$$\frac{a_0}{a_n} = \prod_1^n z_i$$

$$\frac{b_0}{b_m} = \prod_1^m p_i.$$

Letting

$$\frac{a_1}{a_n} = \sum_1^{n-1} z_{i(n-1)}$$

= sum of the products of z_k's ($k=1, 2, \cdots, n$) taken $(n-1)$ at a time

$$\frac{b_1}{b_m} = \sum_1^{m-1} p_{i(m-1)}$$

= sum of the products of p_k's ($k=1, 2, \cdots, m$) taken $(m-1)$ at a time.

Equation (2) becomes

$$\frac{\prod_1^m p_i}{\prod_1^n z_i} = \frac{\sum_1^{n-1} z_{i(n-1)}}{\sum_1^{m-1} p_{i(m-1)}}.$$

Dividing each side by $\prod_1^m p_i / \prod_1^n z_i$ we obtain

$$\frac{\sum_1^m \frac{1}{p_i}}{\sum_1^n \frac{1}{z_i}} = 1.$$

But the given VTF is LPS and therefore $z_i > p_i$, $i = 1, 2, \cdots, n$, and thus

$$\sum_1^m \frac{1}{p_i} > \sum_1^n \frac{1}{z_i}.$$

Hence the above result cannot hold.

Hence $b_0/a_0 < b_1/a_1$. By the same argument, it can be proved $b_2/a_2 < b_1/a_1$ and so on, or

$$\frac{b_i}{a_i} \le \frac{b_{i+1}}{a_{i+1}}, \qquad i = 0, 1, \cdots, (n-1). \tag{3}$$

When $i = n, n+1, \cdots, m$, the inequalities will be replaced by equalities since each term becomes infinity. Hence the theorem is proved.

It may be noted that the coefficient conditions (3) are necessary in the case of *RC*-impedance functions also [1].

Corollary 1: An HPS of an *RC*–LN remains HPS under PD, while an HPNS need not remain so under PD.

Corollary 2: A necessary condition for the coefficients of the VTF of an HPS

$$\frac{Ks^{m-n} \sum_0^n a_{i+m-n} s^i}{\sum_0^m b_i s^i} \quad \text{is} \quad \frac{a_i}{b_i} > \frac{a_{i-1}}{b_{i-1}}.$$

The above two corollaries follow directly from Theorems 1 and 2 by making s to $1/s$ transformation.

It may be noted that the coefficient conditions of Corollary 2 are necessary in the case of *RC* admittance functions also [1].

The results obtained in the paper can be obtained for any two-element-kind network by the familiar transformation.

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Realization of the *A*-Matrix of *RLC* Networks

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***Abstract*—A new theory is proposed for the realization of the *A*-matrix of *RLC* networks, based on the synthesis of *Z*-, *Y*-, and *K*-matrices of multiport resistive networks.**

I. Introduction

The problem of realization of the *A*-matrix of *RLC* networks has been considered by many authors [1]–[10]. Rauch [3] and Yarlagadda and Tokad [4] have dealt with two-element-kind networks having no circuits of capacitors only and no cutsets of inductors only. Dervisoglu's procedure [5] is applicable to the class of *RLC* networks satisfying, in addition to the above assumptions, the condition that the resistive part is connected. In this procedure a new theory is proposed for the *A*-matrix synthesis of *RLC* networks, where the resistive part need not be connected.

II. Formulation and Properties of the *A*-Matrix of *RLC* Networks

Consider an *RLC* network N_{RLC}. From N_{RLC} we obtain the networks N_R, N_{RL}, N_{LC}, and N_{RC} defined as follows: N_R-network obtained by open-circuiting all the inductances and capacitances;

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$N_{RL}(N_{RC})$-network obtained after short-circuiting (open-circuiting) all the capacitances (inductances); N_{LC}-network obtained after open-circuiting all resistances. Further, we make the following assumptions: 1) N_{RLC} is connected and nonseparable; 2) N_{LC} is connected; 3) in N_{RLC} there exists no circuit of capacitances only and no cutset of inductances only. It follows from these assumptions that N_{RC} and N_{RL} are also connected.

Let H be the hybrid matrix of N_R considered as a multiport network for which the terminals of each inductance (capacitance) define a current (voltage) port. If $L(C)$ refers to the diagonal matrix of inductances (capacitances), then the A-matrix of N_{RLC} will be given by

$$A = -\begin{bmatrix} L^{-1} & 0 \\ 0 & C^{-1} \end{bmatrix}\begin{bmatrix} H_{11} & H_{12} \\ -H_{12}^t & H_{22} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}. \quad (1)$$

Let $n_l(n_c)$ represent the total number of inductances (capacitances) of N_{RLC}. Let v_L denote the number of vertices of the network N_{LCs} obtained from N_{LC} after short-circuiting all the capacitances. Let N_R be in p_c parts. Then the following theorem can be established [11].

Theorem 1: a) Rank of $A_{11} = v_L - 1$; b) rank of $A_{22} = n_c - p_c + 1$.

Let a matrix $A = [a_{ij}]$ as partitioned in (1) satisfy the following conditions: 1) $a_{ij} = 0$, if $a_{ji} = 0$; 2) sign matrices of A_{11} and A_{22} are symmetric; 3) sign matrix of A_{12} is the negative transpose of that of A_{21}; 4) $|a_{ij}|/|a_{ji}| \times |a_{jk}|/|a_{kj}| = |a_{ik}|/|a_{ki}|$ for all a_{ij}, a_{jk}, and $a_{ik} \neq 0$. It can be shown that the matrix A can be decomposed as $A = -DH$ where D is diagonal with positive diagonal entries and H is as in (1).

If in N_{RLC} there exists a path consisting of capacitances only between the vertices of an inductance, then the corresponding row, say row i, of $A_{11}(H_{11})$ will consist of zeros only. Further, row i of $A_{12}(H_{12})$ will consist of $0, X, -X(0, -1, 1)$ only where X is a positive constant, and hence $d_i = X$. Once the subgraph consisting of the capacitances of N_{RLC} is known, then the position of such an inductance can be determined using the relevant rows of H_{12}. Hence, in the discussions to follow it is assumed that there are no zeros in H_{11}. This, of course, involves no loss of generality.

III. Synthesis of the Z-Matrix of Resistive n-Port Networks

Given a real symmetric matrix

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$$

let the rank of Z be r and let $[Z_{11}Z_{12}]$ be a submatrix of Z formed by a set of r linearly independent rows of Z, with Z_{11} nonsingular. If $[Z_{21}Z_{22}] = M[Z_{11}Z_{12}]$, where each entry of M is either 0, 1, or -1, then the following procedure may be used to obtain a realization, if one exists, of Z as the open-circuit impedance matrix of a resistive n-port network having a connected port structure [11]. 1) Realize Z_{11}^{-1} as the short-circuit conductance matrix of an r-port network N_r having a connected port structure T. 2) If the entries of M are consistent with the orientation of the ports of N_r, then the ports corresponding to Z_{22} can be located with respect to T. 3) The n-port network obtained by adding to N_r the ports corresponding to Z_{22} will realize Z.

IV. Synthesis of the Hybrid Matrix of a Resistive n-Port Network

Consider a resistive n-port network N. If in N there exists no circuit of voltage ports only and no cutset of current ports only, then the hybrid matrix H of N will exist. If $V_1(V_2)$ and $I_1(I_2)$ refer, respectively, to the vectors of voltages and currents of current (voltage) ports, then

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ -H_{12}^t & H_{22} \end{bmatrix}\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = H\begin{bmatrix} I_1 \\ V_2 \end{bmatrix}. \quad (2)$$

Let the graph of voltage ports of N be in p parts, $T_1, T_2, \cdots, T_p$. Construct on N another n-port network N^* such that 1) the resistive part of N^* is the same as that of N, 2) the graph of the current ports of N^* is the same as that of N, and 3) the graph T^* of the voltage ports of N^* is in p parts, $T_1^*, T_2^*, \cdots, T_p^*$ with each T_i^* constructed on the vertices of the corresponding T_i. If V_1^*, V_2^*, I_1^*, I_2^*, and H^* refer to the quantities of N^* corresponding to V_1, V_2, I_1, I_2, and H of N, then

$$\begin{bmatrix} V_1^* \\ I_2^* \end{bmatrix} = \begin{bmatrix} H_{11}^* & H_{12}^* \\ -H_{12}^{*t} & H_{22}^* \end{bmatrix}\begin{bmatrix} I_1^* \\ V_2^* \end{bmatrix}. \quad (3)$$

Let

$$V_2 = Q\,V_2^*. \quad (4)$$

It may be noted that the matrix Q is entirely topological in nature. It can be shown that

$$H_{11}^* = H_{11} \qquad H_{22}^* = Q^t H_{22} Q \qquad H_{12}^* = H_{12}Q. \quad (5)$$

We next consider the synthesis of the hybrid matrix of resistive n-port networks. We make the following assumptions: 1) there exists in the required network N no circuit of voltage ports only and no cutset of current ports only; 2) the graph of ports is connected.

Before we outline the synthesis procedure, we extend the definition of potential factor [12] to include cases where internal vertices, i.e., vertices which are not terminals of any ports, are present. If v_j is an internal vertex, then the potential factor of v_j with respect to a port i is defined as equal to the voltage of v_j with reference to the negative reference terminal of port i when port i is excited with a source of unit voltage and all the other ports are short-circuited. We next discuss the hybrid matrix synthesis procedure.

Given the hybrid matrix H, we first determine the rank of H_{11} and locate a nonsingular principal submatrix $\boldsymbol{H}_{11}$ of order equal to the rank r of H_{11}. Let the first r rows of H_{11} correspond to $\boldsymbol{H}_{11}$. Let the corresponding submatrix of H_{12} be $\boldsymbol{H}_{12}$. We note that the matrix

$$\begin{bmatrix} \boldsymbol{H}_{11} & \boldsymbol{H}_{12} \\ -\boldsymbol{H}_{12}^t & H_{22} \end{bmatrix}$$

is the hybrid matrix of the network which will result if the last $(n_I - r)$ current ports of the required n-port network N are open-circuited, where n_I is the total number of current ports (i.e., the number of rows of H_{11}). The short-circuit admittance matrix Y_A of such a network can be easily determined. We then realize Y_A [13] by a multiport resistive network having a connected port structure. Let such a realization be denoted by N_A. The number of ports of N_A will be $(n_v + r)$ where n_v is the total number of voltage ports (i.e., the number of rows of H_{22}). The port graph of N_A will be the same as the subgraph of the port graph of the required network N, consisting of all the voltage ports and the first r current ports. Hence, from N_A we can determine $T_1, T_2, \cdots, T_p$ and the location of the first r current ports with respect to $T = T_1 \cup T_2 \cup T_3 \cdots \cup T_p$. If $\overline{N_A}$ is obtained from N_A after open-circuiting all the current ports, then T will be the port graph of $\overline{N_A}$. We note that the resistive part of $\overline{N_A}$ is the same as that of the required network N. Thus it only remains to determine the position of the last $(n_I - r)$ current ports.

If G_p is the graph of ports of N, let $\overline{G_p}$ represent the graph resulting from G_p after short-circuiting all the voltage ports. Following the procedure described in the last section, the graph $\overline{G_p}$ consisting of current ports can be determined. Since $T = T_1 \cup T_2 \cdots \cup T_p$ is a subgraph of G_p, in G_p there will be one vertex v_i corresponding to each T_i. Let the first p vertices of $\overline{G_p}$ be designated by $v_1, v_2, \cdots, v_p$, v_i corresponding to T_i. The remaining vertices of $\overline{G_p}$ will be the internal vertices of $\overline{N_A}$.

If N^* is the n-port network constructed on N such that each T_i^* is a Lagrangian tree, then the matrix Q and hence $H_{12}^* = H_{12}Q$ can be evaluated. Let G_p^*, $\overline{G_p^*}$, T^* represent graphs of N^* corresponding to the graphs G_p, $\overline{G_p}$, and T of N. It should be noted that $\overline{G_p^*}$ and $\overline{G_p}$ are identical and $G_p^* = \overline{G_p} \cup T^*$. Further, H_{12}^* represents the voltage across the current ports of N^* when the voltage ports of N^* are excited and the current ports are open-circuited. Hence, $\boldsymbol{H}_{12}^*$, the submatrix of H_{12}^* corresponding to the first r ports, will determine uniquely the potential factors of $\overline{N_A^*}$.

Let a current port m, $m > r$, be incident in $\overline{G_p}$ between the vertices v_i and v_j, $i, j \leq p$. Then in $\overline{N_A}$, one of the terminals of this current port will be in T_i^* and the other in T_j^*. If $i \leq p$ and $j > p$, then one of the terminals of the current port m will be in T_i^* and the other will be the internal vertex of $\overline{N_A^*}$, corresponding to the vertex v_j of $\overline{G_p}$. In both cases the position of the current port in G_p^*, and hence in G_p, can be determined using $\overline{H_{12}^*}$, which is the submatrix formed by the last $(n_I - r)$ rows of H_{12}^*. If both i and j are greater than p, then the position in $G_p^*(G_p)$ of the current port m is the same as its position in $\overline{G_p^*}(G_p)$. This way all the current ports can be located in G_p.

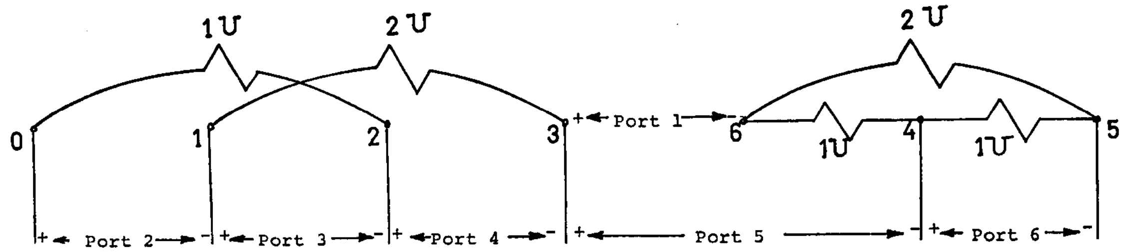

Fig. 1.

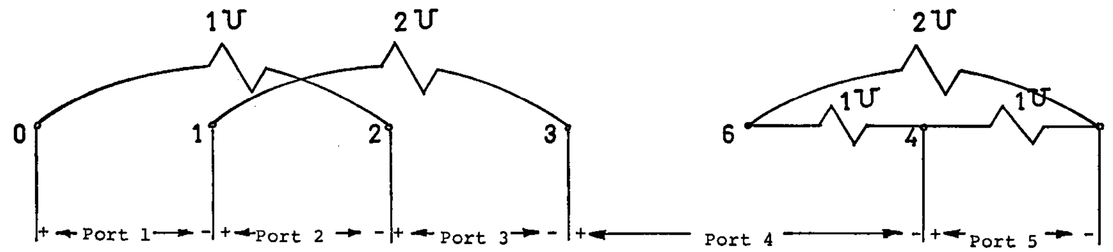

Fig. 2.

It should be emphasized that in determining the last $(n_I - r)$ current ports only some entries of H_{12}^* will be required. Hence, it is necessary to check whether the remaining entries of H_{12}^* are consistent with the potential factors of N_A and the graph G_p^*.

V. Realization of the A-Matrix

Realization of the A-matrix of RLC networks as seen from the above discussions consists of the following steps: 1) decomposition of A as $A = -DH$; 2) realization of H as the hybrid matrix of a resistive n-port network.

In the case of the realization of the A-matrix of $RC(RL)$ networks, we will be required to realize instead of a hybrid matrix H a short-circuit (open-circuit) conductance (resistance) matrix. Thus we have the following theorem.

Theorem 2: If a real $(n \times n)$ matrix $-A$ is realizable as the short-circuit (open-circuit) conductance (resistance) matrix of a resistive n-port network, then A will be realizable as the A-matrix of an $RC(RL)$ network.

For the case of RC networks, a result more general than that of Theorem 2 can be obtained, as seen from the next theorem.

Theorem 3: Let A be a real matrix with all diagonal entries negative. Let $A = [a_{ij}]$ satisfy the following conditions: 1) $-A$ is dominant; 2) $a_{ji} = 0$ if $a_{ij} = 0$; 3) sign pattern of A is symmetric; 4) $|a_{ij}|/|a_{ji}| \times |a_{jk}|/|a_{kj}| = |a_{ik}|/|a_{ki}|$ for all a_{ij}, a_{kj}, and a_{ik} not equal to zero. Then A is realizable by an RC network.

Proof: The matrix A satisfying conditions 2)–4) can be decomposed as $A = -DY$ where D is diagonal with all diagonal entries positive and Y symmetric with positive diagonal entries. Since $-A$ is dominant, Y will also be dominant. Hence, Y can be realized as the short-circuit conductance matrix of a $2n$-node n-port network N [14]. Replacing the ports of N by capacitances whose values are determined by the diagonal entries of D will result in a realization of the A-matrix.

Example: It is required to realize the matrix given A below:

$$A = -\left[\begin{array}{rr|rrrrr} 1 & -1 & 0 & -3 & -3 & -3 & -2 \\ -1 & 1 & 0 & 0 & 0 & 3 & 2 \\ \hline 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 3 & 2 & 0 & 0 \\ 1 & 0 & 0 & 2 & 2 & 0 & 0 \\ 3 & -3 & 0 & 0 & 0 & 0 & 0 \\ 2 & -2 & 0 & 0 & 0 & 0 & 5 \end{array}\right] = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}.$$

The matrix A is partitioned as indicated above to ensure that the sign matrices of A_{11} and A_{22} are symmetric and the sign matrix of A_{12} is the negative transpose of that of A_{21}. A can be decomposed as

$$A = -\begin{bmatrix} 3 & & & & & & \\ & 3 & 0 & & & & \\ & & 1 & & & & \\ & & & 1 & & & \\ & & & & 1 & & \\ & & & & & 3 & \\ & & & & & & 3 \end{bmatrix} \left[\begin{array}{rr|rrrrr} 1/3 & -1/3 & 0 & -1 & -1 & -1 & -2/3 \\ -1/3 & 1/3 & 0 & 0 & 0 & 0 & 2/3 \\ \hline 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 3 & 2 & 0 & 0 \\ 1 & 0 & 0 & 2 & 2 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 2/3 & -2/3 & 0 & 0 & 0 & 0 & 5/3 \end{array}\right]$$

$$= -[D]\begin{bmatrix} H_{11} & H_{12} \\ -H_{12}^t & H_{22} \end{bmatrix}.$$

Let the first two rows of $A(H)$ correspond to inductances (current ports) and the last five rows of $A(H)$ correspond to the capacitances (voltage ports) of the network (7-port network) N realizing $A(H)$. Let the ith row of H correspond to the port i of the 7-port network N.

The matrix obtained after crossing out the first row and the first column of H is the hybrid matrix of the network which will result after the first current port of N is open-circuited. The short-circuit conductance matrix Y_A of such a network is given by

$$Y_A = \left[\begin{array}{r|rrrrr} 3 & 0 & 0 & 0 & -3 & -2 \\ \hline 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 3 & 2 & 0 & 0 \\ 0 & 0 & 2 & 2 & 0 & 0 \\ -3 & 0 & 0 & 0 & 3 & 2 \\ -2 & 0 & 0 & 0 & 2 & 3 \end{array}\right].$$

The 6-port network N_A realizing Y_A is shown in Fig. 1. The ith row (port) of $Y_A(N_A)$ corresponds to port $i+1$ of N. The port graph of N_A is the same as the subgraph of the port graph of N consisting of the second current port and all the voltage ports. $\overline{N_A}$, the 5-port network obtained after open-circuiting the current port of N_A, is shown in Fig. 2. Vertex 6 is the internal vertex of $\overline{N_A}$. Port i of $\overline{N_A}$ is the same as port $i+2$ of N.

Since all the entries of H_{11} are equal in magnitude, the current ports of N will come in parallel after all the voltage ports of N are short-circuited. From this it follows that vertex 6 will be a terminal of current port 1 and the other terminal of this port remains to be determined. It should be noted that the port graph of $\overline{N_A}$ is in one part.

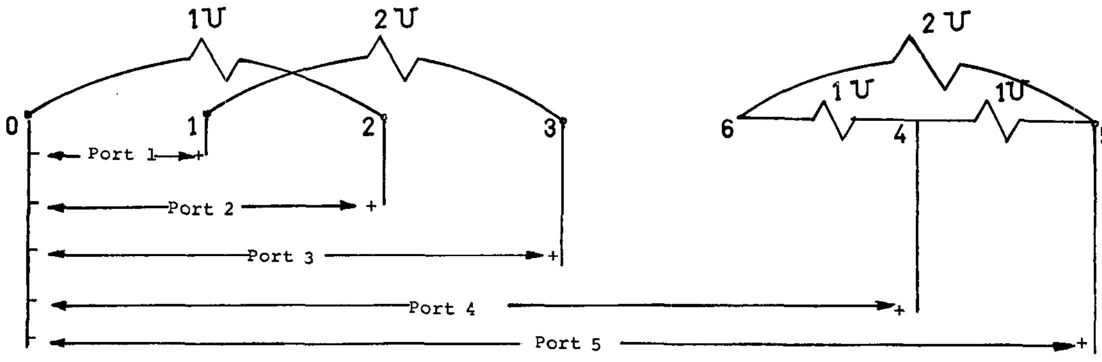

Fig. 3.

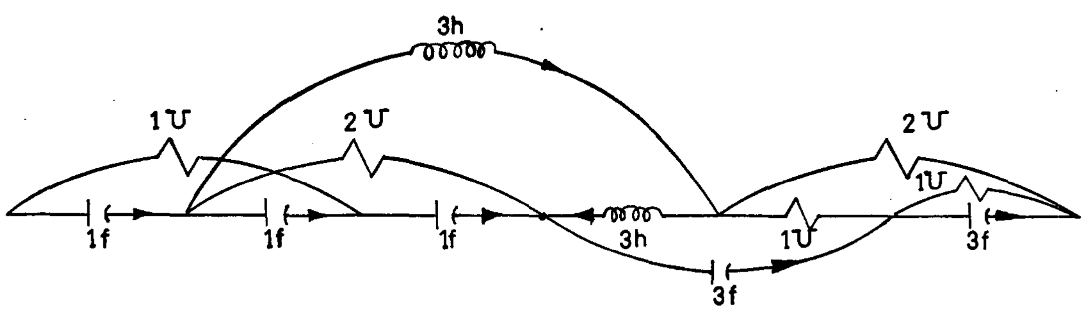

Fig. 4.

Let $\overline{N_A}^*$ be as shown in Fig. 3. The matrix Q is obtained as

$$Q = \begin{bmatrix} -1 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 & -1 \end{bmatrix}.$$

Then

$$H_{12}^* = H_{12}Q = \begin{bmatrix} -1 & 0 & 0 & 1/3 & 2/3 \\ 0 & 0 & 1 & -1/3 & -2/3 \end{bmatrix}.$$

Using the second row of $\underline{H_{12}}^*$ the potential factors K_{i_6} of vertex 6 with respect to port i of $\overline{N_A}^*$ are obtained as follows:

$$K_{16} = 0 \quad K_{26} = 0 \quad K_{36} = 0 \quad K_{46} = 1/3 \quad K_{56} = 2/3.$$

Then from the (1×1) entry of H_{12}^* it can be seen that vertex 1 is the second terminal of the first current port of N and the positive reference terminal of the port is at vertex 6. The network N realizing the matrix A is then obtained as shown in Fig. 4. It should be noted that the resistive part of N is in three parts.

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Passive Network Realization Using Abstract Operator Theory

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This correspondence concerns the very strong connection which exists between realizability theory for lossless networks and a branch of abstract operator theory as studied by mathematicians. Although many mathematicians have been involved in the development of this theory (see for example [1]–[5]), we take the viewpoint of Nagy and Foias. The purpose of this correspondence is to point out that the main passive network realizability theorem as stated in [6, theorem 3.3] when restricted to lossless networks is a special case of a major theorem of Nagy and Foias. Our mathematical Theorems 1 and 2 can be interpreted as synthesis theorems for passive Hilbert ports (see [7] for the definition of Hilbert ports). However, it is only in the lossless case that they coincide with ordinary n-port synthesis theorems. We also note that the methods of proof are constructive. A lengthier discussion of these results will appear in [8] and this reference is recommended to the interested reader.

The fact that a connection exists between modern operator theory and electrical engineering has been known for several years. In [9], Livsic worked out the connection between his approach to characteristic functions for operators and network realizability theory. Unfortunately, this book has not been translated into English and its circulation in this country is small. The viewpoint of the present correspondence is not that of Livsic, and the approach taken here appears to be new to electrical engineers and mathematicians. The author has recently learned that independently and concurrently DeWilde has begun to use this same type of mathematics to study network synthesis [10]. His approach is somewhat different from this one. We begin by stating precisely the mathematical theorems involved.

Let H be a complex Hilbert space with inner product $(\ , \ )$ and let $\mathcal{L}(H)$ denote the space of bounded linear operators on H. For example, if H were the space of n-tuples with complex entries, then $\mathcal{L}(H)$ would be the $n\times n$ matrices with complex entries. If A is an operator in $\mathcal{L}(H)$, then A^* will denote its Hermetian adjoint. Recall that $\|x\|$ is $\sqrt{(x, x)}$ if $x \in H$. We also assume that H is the complexi-

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