AME 3623: Embedded Real-Time Systems: Final Exam
Solution Set
May 13, 2005

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<th>Topic</th>
<th>Max</th>
<th>Grade</th>
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1. Logic

Given the following function:

<table>
<thead>
<tr>
<th>A B C D</th>
<th>f</th>
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<tr>
<td>0 0 0 0</td>
<td>1</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>1</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>1</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>1</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>1</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>0</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>1</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>1</td>
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<tr>
<td>1 0 0 0</td>
<td>1</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>1</td>
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<tr>
<td>1 0 1 0</td>
<td>1</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>1</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>1</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>0</td>
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<tr>
<td>1 1 1 0</td>
<td>1</td>
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<tr>
<td>1 1 1 1</td>
<td>1</td>
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(a) (10 pts) Show the Karnaugh map and the clusters.

<table>
<thead>
<tr>
<th>AB</th>
<th>CD</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00</td>
<td>1 1 1 1</td>
</tr>
<tr>
<td>01</td>
<td>01</td>
<td>1 0 0 1</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
<td>1 1 1 1</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>1 1 1 1</td>
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</table>
(b) (7 pts) What is the algebraic expression for the corresponding circuit?

\[ f = \overline{BCD} \]

(c) (7 pts) Show the circuit
Given the following circuits:

(d) (15 pts) Show the corresponding truth table for $D_0$ and $D_1$.

<table>
<thead>
<tr>
<th>$E$</th>
<th>$X_1$</th>
<th>$X_0$</th>
<th>$D_1$</th>
<th>$D_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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</tbody>
</table>
Given the following sequential logic circuit (note its relationship to the circuits in the previous problem):

(e) (8 pts) Assume an initial condition of $X1 = 0 \ X0 = 1$, and that $E = 1$. Show the timing diagram for 4 clock cycles (include $X1$, $X0$ and $CLK$).
(f) (8 pts) Assume an initial condition of $X_1 = 1$ $X_0 = 1$, and that $E = 0$. Show the timing diagram for 4 clock cycles (include $X_1$, $X_0$ and $CLK$).

![Timing Diagram]

(g) (5 pts) From the perspective of a Finite State Machine representation of this circuit, what are the events/inputs?

*The events are UP ($E=1$) and DN ($E=0$), and arrive on the upward transition of the clock.*

(h) (10 pts) Show the state transition diagram.

![State Transition Diagram]
2. **Arithmetic**

Consider the following decimal numbers: $X = 38$ and $Y = 47$

(a) (7 pts) What is the two’s complement binary representation of $-Y$ (assume an 8 bit representation)?

$47 = 00101111$

so:

$-47 = 11010001$

(b) (8 pts) In binary, subtract $Y$ from $X$ (show your work).

$38 = 00100110$

So:

\[
\begin{array}{c@{}c@{}c@{}c@{}c@{}c@{}c@{}c@{}c}
 & & 0 & 0 & 1 & 0 & 0 & 1 & 1 & 0 \\
+ & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 1 \\
\hline
= & 1 & 1 & 1 & 1 & 0 & 1 & 1 & 1 & 1 \\
\end{array}
\]

(The decimal equivalent of this result is $-9$.)
3. Microprocessor Design (30 pts)

(a) (5 pts) What is the function of the ALU?

*The Arithmetic Logical Unit performs (as the name suggests) arithmetic (e.g., add, subtract, multiply, divide) and logical (e.g., and, or, xor) operations on individual or pairs of binary operands.*

(b) (5 pts) What is the function of the program counter?

*The program counter contains the address of the memory location that contains the instruction that is currently being executed.*

(c) (10 pts) Give two examples of signals generated by the instruction decoder.

- Addresses for the registers to be used in the next operation.
- Control signals for the ALU.
- Control and addressing signals for the memory.
- Signals that affect the status register.

(d) (5 pts) Explain (in brief) the function of the “chip select” signal in a memory circuit.

*The chip select signal is used to select an entire memory chip (or module) for a read or write operation. When selected, the state of the module may be altered (in a write operation) or the module may drive the data bus (in a read operation). This type of implementation allows one to have multiple memory modules on the same data bus.*

(e) (5 pts) Explain (in brief) the function of the clock signal in a memory circuit.

*The clock signal indicates the instant that a write operation is to take place from the data bus into a memory element. Prior to this instant, the memory address must have already been set up.*
4. **Interrupts and I/O** (33 pts)

(a) (5 pts) True/false: in pulse-width modulation control, information is encoded in the frequency of the signal.

False. *Information is encoded in the duty cycle of the signal.*

(b) (7 pts) For the given clock rate and prescaler configuration of the mega8 timer0, give the time (in microseconds) between timer increments (reduced fractions are fine, where necessary).

<table>
<thead>
<tr>
<th>Prescaler</th>
<th>1 MHz clock</th>
<th>16 MHz clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>No prescaler</td>
<td>1µs</td>
<td>1/16µs</td>
</tr>
<tr>
<td>Div 8</td>
<td>8µs</td>
<td>1/2µs</td>
</tr>
<tr>
<td>Div 64</td>
<td>64µs</td>
<td>4µs</td>
</tr>
<tr>
<td>Div 256</td>
<td>256µs</td>
<td>16µs</td>
</tr>
<tr>
<td>Div 1024</td>
<td>1024µs</td>
<td>64µs</td>
</tr>
</tbody>
</table>

(c) (5 pts) Assume that we configure timer0 so that it uses a prescaler of 64 and produces an interrupt. Also assume a clock frequency of 16MHz. How often will an interrupt be generated?

\[4\mu s \times 256 = 1024\mu s \approx 1\text{ms}\]
(d) (8 pts) What effect does the following code have on the state of this circuit (in terms of flip-flop state)? What effect does this state change have?

```c
DDRB &= 4;
```

*This one was unintentionally tricky: this does not change the state of flip-flop A (for PB2), but it does set the state of all of the other pins such that they are all inputs.*
(e) (8 pts) What effect does the following code have on the state of this circuit (in terms of flip-flop state)? What effect does this state change have?

```
PORTB &= 0xFB;
```

*This operation sets the output state of the pin to 0 (by setting the state of flip-flop B to 0). If this port is configured as an output port, then the pin is set to a low state.*
5. Serial Communication

(a) (10 pts) Explain why we do not use a start bit value of “1” in our infrared serial implementation.

In our implementation, a “1” would be encoded with no signal. This choice would mean that the receiver could not distinguish between a start bit and nothing being transmitted. As a result, the receiver would have no timing information with which to synchronize with the transmitter.

(b) (5 pts) Does the receiver or the sender compute the checksum value?

*Both sides compute the checksum. (it is the receiver that compares the sent checksum with its own computation of the checksum)*

(c) (5 pts) True/False: a UART can perform byte-level error correction and detection.

*True*

(d) (5 pts) True/False: a UART can perform packet-level error correction and detection.

*False. Packet-level communication is application-specific; the UART is focused on application-independent communication.*

(e) (5 pts)

Consider a packet that contains the following values: 0x45, 0x12, 0xFA. What is the checksum value?

*0x51 (we drop the carry)*
6. **Bonus** (2 pts)

   What is the magic number?

   $0xF3$
7. Finite State Machines

Below is the state transition diagram of the vending machine that we designed in class. Recall that once the machine receives $.20 (composed of nickels and dimes), it will respond to a button press by dispensing the requested drink (Jolt or Buzz Water). Redesign this FSM to add the following “Easter Egg” feature:

Starting from the $0 state, if the user inserts the following coins in this specific order: nickel, dime, nickel, the machine immediately returns the three coins and is ready to dispense a drink and an additional nickel.

Where the events are: N = Nickel (insertion); D = Dime (insertion); J = Jolt (request); BW = Buzz Water (request).

And the actions are: RN = Return Nickel; RD = Return Dime; DJ = Dispense Jolt; DBW = Dispense Buzz Water; Z = no action.
Hint: in order to implement the Easter Egg feature, you will need to add additional states and state transitions.

(a) (5 pts) What are the states in this new FSM?

$0, \$0.05, \$0.15, \$0.15EE, \$0.20, \text{ and } \$0.20EE \text{ (where “EE” stands for Easter Egg). We introduced these new states to distinguish between arriving at 20 cents in the special sequence and arriving in any other sequence.}

(b) (5 pts) What are the actions in this new FSM?

- Dispense nickel (RN)
- Dispense dime (RD)
- Dispense Jolt (DJ)
- Dispense Buzz Water (DBW)
- * Dispense two nickels and a dime (may not be necessary depending on the FSM design). (NDN)
- * Dispense Jolt and a nickel (same goes for this action). (DJ-RN)
- * Dispense Buzz Water and a nickel (same). (DBW-RN)
- Nothing (Z)

I will accept the list without the starred items.
(c) (10 pts) Show the state transition diagram (if you choose, you may modify the diagram on the previous page).