Performance of Multiple-Bus Multiprocessor Under Non-Uniform Memory Reference Model

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ABSTRACT

Performance evaluation of multiple-bus multiprocessor systems is usually carried out under the assumption of uniform memory reference model. Hot spots arising in multiprocessor systems due to the use of shared variables, synchronization primitives etc., give rise to non-uniform memory reference patterns. The objective of this paper is to study the performance of multiple bus multiprocessor system in the presence of hot spots. Analytic expressions for the average memory bandwidth and probability of acceptance of prioritized processors have been derived. The results are validated by simulation results. Keywords: Multiple bus interconnection, performance evaluation, memory bandwidth, blocking probability, multiprocessors.

Seamless - A Latency-Tolerant RISC-Based Multiprocessor Architecture

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ABSTRACT

The Seamless parallel system being developed at the University of Iowa ECE Department provides a method for providing latency tolerance in physically-distributed memory systems utilizing “off-the-shelf” RISC CPUs without incurring the overhead of multithreading. Seamless encompasses an evolutionary new programming model emphasizing data locality that views communication as data movement rather than message passing I/O. A hardware Locality Manager is added to each processing element to perform this data movement concurrently with computation.