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A DSP-based microcomputer system for echo measurement in telephone networks

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A schematic design is presented for a stand-alone test device to measure all aspects of echo at the subscriber location of dial lines in telephone networks. The proposed architecture is based on off-the-shelf components such as a general purpose PC and one of the available digital signal processing (DSP) boards with minimum additional hardware. Echo aspects are identified for measurements and the firmware (both hardware and software) of the design are presented. Although specific hardware components are chosen in the proposed system, the strategy of the design can account for different components. The system is tested in the laboratory using a telephone channel simulator under different conditions. It is also used in real telephone circuits. Samples of testing results are included.

1. Introduction

Since the development of the digital computer, there has been a great demand for a means of linking two or more computers with each other. A significant amount of research has been devoted to the development of computer and data networks (Bertsekas and Gallagher 1987). For any network, there is a need for a transmission medium through which the information can pass. Obviously, most attention has been focused on telephone networks since wires have been installed almost everywhere. However, owing to bandwidth limitations and other impairments, dedicated links have been provided. Needless to say, these links are expensive and the number of interconnected terminals is limited. Consequently, it would be desirable if one could utilize the existing telephone exchange facilities. Therefore, modem design has evolved quite rapidly in order to achieve high data rates via telephone channels (Tannenbaum 1981, Falconer and Gitlin 1984). It is now possible to transmit in full duplex mode 19 200 and 14 400 bits per second on leased and dial lines, respectively. The latter is achieved through the use of echo cancellation, where the entire channel bandwidth is used simultaneously for both transmit and receive signals. The first commercial echo canceller modem became available only in 1987. It is a CCITT (Comité Consaultatif International Télégraphique et Téléphonique) V.32 standard and is finding increasing application in fast full-duplex data transmission systems over the general switched telephone network (GSTN) (Werner 1984, Wang and Werner 1988). In fact, the intent is to increase the rate to a point very close to the channel capacity limit of nearly 28 000 bits per second over GSTN. The CCITT is still working on this. The advances in signal processing and digital communications fields have led the way towards the achievement of this goal (Falconer and Gitlin 1984).

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The performance of echo cancellers depends on the characteristics of the echo under consideration. For example, an optimum canceller for the U.S. telephone network has been found to suffer from degradation when used in the U.K. network, and vice versa (El-Hannawey and Zaidan 1992). Therefore, extensive echo testing is required in all telephone networks to determine the best type of canceller to use on a particular line. Modem manufacturers tailor their design by testing cancellers mainly in North America and Europe. This is primarily due to the large number of telephone-based data networks in these two continents.

Telephone network performance varies from one country to another. In fact, it varies within the same country. These variations are due to the different levels of impairment associated with each line in the network. Among these variations are channel attenuation, additive white noise and impulsive noise, amplitude and delay disortions, amplitude and phase hits and finally, echo which is restricted to dial lines. Prior to the determination of the data rate that a network can handle, measurements of the above impairments are necessary. Although there exists a variety of test equipment from various manufacturers to measure the above impairments, there is no equipment available for measuring different aspects of echo. Since the goal is to utilize dial lines of the telephone network for data transmission at the maximum possible rate, such equipment is really needed for manufacturers, carriers and network establishments. It is the intent of this paper to propose the design of such equipment for echo measurement where all aspects of echo are identified. An effort has previously been made by Wittke *et al.* (1984) to measure the echo in GSTN. Their approach was based on collecting the data, storing it, then processing it at a later stage on a mainframe computer. In contrast, the system proposed here involves stand-alone echo measurement equipment based on a general purpose micro-computer armed with a versatile digital signal processing board with minimal additional hardware. Being completely programmable, the system components (i.e. the PC and the digital signal processing—DSP—board) can be configured to perform several other functions while the system is not being used as an echo measurement device.

In § 2 of this paper, we present different echo parameters to be measured. Various echo model structures can be used and implemented on a digital signal processor. The data driven or interpolating structure is the most preferable because it is accurate and easy to implement (Werner 1984). The structure of this model and the echo measurement strategy is described in § 3. Finally, in § 4, we propose the firmware (hardware and software) and the specifications of the new equipment.

2. Echo parameters

The subscriber loop (connecting the subscriber to his nearest central office 'CO') is made of two wires (one pair) simultaneously carrying the two signals in both directions. Signals are separated at the two ends, the subscriber and the central office, by means of a hybrid, as shown in Fig. 1. The hybrid is a device that provides isolation between the transmit and received signals in full duplex transmission. Echoes are generated in telephone networks whenever the transmitted signal encounters a coupling hybrid at the 4-wire to 2-wire connections caused by the impedance mismatch of the line (Werner 1984). Obviously, owing to the variations of line characteristics and possible switched connections there is no unique line impedance.

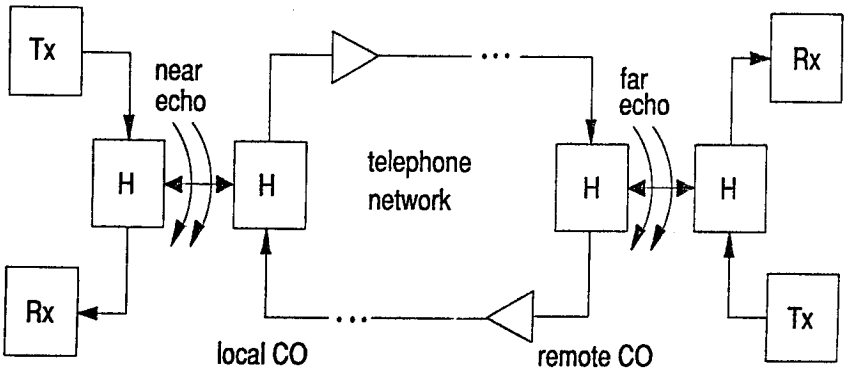

Figure 1. Near and far echo.

The echo signal consists primarily of two components. The first component, called local echo or near echo, is due to the reflection of the transmit signal at the local subscriber hybrid and the hybrid of the near central office. The second component, called remote or far echo, is due to reflection at the corresponding hybrids of the remote end of the call as shown in Fig. 1. The echo received due to the transmit signal as a source is called talker echo, where the talker hears his own echo. Owing to the possibility of multiple reflections, the echo signal may be received at the remote end. In this case it is called listener echo, which is a delayed and distorted replica of the desired signal to be received. Talker echo may also include other components due to multiple reflections. Normally, these components are relatively weak because of channel attenuation. Usually, there is a delay between the near and the far echo components. This delay ranges from a few milliseconds for short-haul connections up to several hundred milliseconds for satellite links, and is called the round-trip delay (Guidoux and Peuch 1984).

The near and far echoes are characterized by their amplitude and dispersion. Signal levels at different positions in GSTN networks are governed by the local authority of the carrier. In most cases it is the ministry of Posts, Telephony and Telegraphy (PTT) (in European countries) or the local carrier company (in North America). In general, the transmit signal power ranges from -10 to 0 dBm, whereas the received signal power is from -40 to -25 dBm. Taking into consideration the insertion loss of the hybrid, which is about 10 dB, the near echo signal has a power range of -20 to -10 dBm. On the other hand, the far echo is normally much lower than the transmitted signal. Although there is no universal measure of the far echo (owing to the very wide variety of possible switching connections), it is always much smaller than the near echo. In most cases, the far echo is even smaller than the received signal. Dispersion is more noticeable in the far echo.

The far echo may suffer some phase rolling, when non-coherent analogue carrier systems are used within the connection (Wang and Werner 1988). A frequency offset is generated due to the modulation and demodulation processes. No matter how small the frequency offset is, phase roll should be compensated for because the adaptation rate of the coefficients of the canceller is extremely small in the data mode. While frequency offset normally lies in the neighbourhood of 0·1 Hz, it may reach a value of 3–4 Hz in Europe (Werner 1985). According to the CCITT

recommendations (V Series), the data modems should be able to handle frequency offsets up to 7 Hz. Therefore, the frequency offset is another important echo parameter to measure. In summary, the different echo parameters to be measured are the amplitude and time dispersion of both the near and far echo impulse responses, the round-trip delay, and the frequency offset. The design of the test device should account for all possible extremes of these measured quantities.

3. Echo model and measurements strategy

The most general echo model structure is the complex FIR tapped delay line filter, with coefficients equal to the sampled impulse response of the echo channel. Of the various structures proposed to implement that filter, the pass-band data-driven or interpolating filter is most preferable because of its accuracy and its implementation simplicity (Werner 1984). In this case, the input is the complex rotated (modulated) data symbols whereas the output is real. The model consists of two sections, the near part and the far part, separated by a bulk delay. The sampled impulse response of the echo channel is synthesized at the transmitter using the above filter which is referred to as an echo canceller. The echo canceller generates an estimate of the received echo signal. The error between the actual received echo signal and the synthesized one is used to update the echo canceller coefficients by an adaptation scheme. Because of its suitability in real time applications, the least mean square (LMS) algorithm is usually used (Haykin 1986). The only price to pay for the simplicity is the longer convergence time. However, the overall duration of a testing call lasts for a few minutes, while accuracy is maintained.

3.1. *The echo channel impulse response*

As previously stated, one of our objectives is to measure the time dispersion of the echo channel. The elements of the proposed system are shown in the functional block diagram of Fig. 2 (Werner 1984). The error signal is also used for activating the phase-lock loop for frequency offset measurement.

The first element of the system produces a stream of binary bits of 0's and 1's at 4800 bits per second, which is the output of a pseudo-noise (PN) generator to ensure a flat spectrum over 600–3000 Hz. The QPSK signalling scheme is used. In this scheme, we have four symbols located at different points in the signal constellation. Every two consecutive binary bits are represented by one point. Accordingly, the output of the encoder consists of the in-phase and the quadrature components. These components have values of ± 1 at 2400 bauds which is the symbol rate. A carrier frequency of 1800 Hz is used to modulate the in-phase and quadrature components. These values are in the CCITT's V.32 recommendation for the first echo-canceller modem. Because of the convenient relationship between the carrier frequency and the baud rate, the modulation simply becomes a process of rotating the symbols in the signal space. The values of the rotated symbols are ± 1 and these symbols are fed to the transmitting filter as well as the echo canceller at a symbol (baud) rate of 2400 symbols per second. The real output of the transmitting filter (obtained at a sampling rate of 7200 samples per second) is converted to analogue using a D/A converter and then applied to an analogue filter to smooth the transmitted signal through the telephone line and to match the PTT specifications. In order to simplify the design, the interpolation technique is used. That is, although the input to both the canceller and the transmit filter is at the symbol rate (2400

baud), the output is obtained at the sampling rate (7200 samples/s), which is three times the symbol rate in this case. This can be simply achieved by using three sub-cancellers, each having the same input, taking the outputs sequentially in a rotating manner (Werner 1984). Each sub-canceller now works independently from the other two. The LMS updating equation used is as follows (Werner 1984):

$$c_k^{(i)}(t+T)=c_k^{(i)}(t)+\alpha\cdot x^*(t-kT)\cdot e(t+iT_s) \tag{1}$$

where $c_k^{(i)}(t)$ is the kth tap coefficient of ith sub-canceller, T is the symbol period, α is the adaptation step size, $x(t)$ is the input to both echo canceller and transmit filter, and $e(t)$ is the error between the received and the synthesized echo signals. The asterisk denotes the complex conjugate operation. Note that the sampling period T_s is one third of the symbol period T, and that the canceller taps $c_k^{(i)}(t)$ and the corresponding input signal $x(t)$ are all complex (the in-phase and quadrature components).

The received analogue echo signal is first fed to an anti-aliasing filter. The output of the filter is sampled at the same rate of 7200 samples per second in synchronism with the transmitted samples. The signal is then converted to digital using an A/D converter. The outputs of the echo canceller (which represents the estimated echo) and the A/D converter are applied to a subtractor. The error between the actual echo signal and the estimated echo is used to update the coefficients of the echo canceller according to the LMS algorithm with adjustable step size as described previously. The time spans of the near and far cancellers are chosen to be 28T (11·67 ms) and 32T (13·33 ms), respectively. These correspond to a total of 180 complex tap coefficients, 84 of which are for the near canceller, while the remaining 96 taps are for the far canceller.

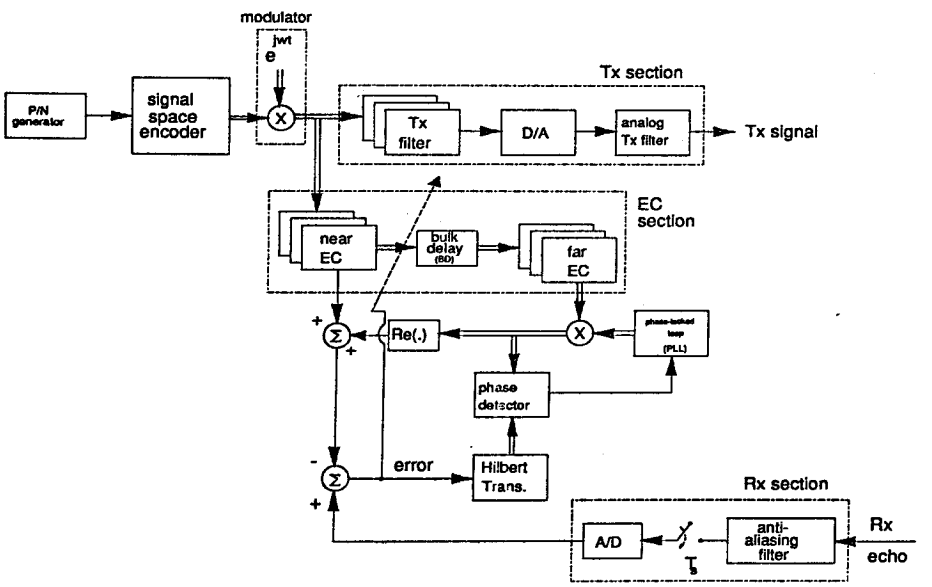

Figure 2. The proposed system functional block diagram.

3.1.1. *Scaling echo channel impulse responses.* The near and far impulse responses (both real and imaginary parts) are displayed on the PC screen adjacent to each other with the measured round-trip delay (and the frequency offset) indicated at the bottom. The size of the near channel impulse response depends on the strength of the near echo component which is normally characterized by the line, whereas the strength of the far echo signal (and consequently the size of the far channel) is an attribute of the switched connection. Since the device is intended for use with different lines at various connections, a wide variety of impulse response sizes is likely to take place. Different scale factors are set by the operator while using the data entry menu for scaling the near and the far impulse responses. These factors are NSCALE and FSCALE. The program uses them according to Fig. 3. Note that the smaller the factor, the larger the impulse response. Since normally the far echo component is weaker than the near one, FSCALE is to be set smaller than NSCALE and consequently the displayed far channel impulse response is expected to flicker more than that of the near.

3.2. *The round-trip delay*

The strategy followed to find the round-trip delay is summarized in the flowchart of Fig. 4. The process begins with the transmission of the standard 2100 Hz answering tone for about 5 s to disable network echo suppressors. Then, a one-tap canceller is inserted to remove any DC quantity from the received signal. Next, we enable only the near canceller update because normally the near echo signal is much stronger than the far echo signal. After leaving ample time for convergence of the near canceller, it is kept frozen. We initially set the bulk delay (BD) to be zero, i.e. the far canceller delay line is filled with data which has just passed that of the near one. The far canceller update is then enabled for 1000 symbol periods (which assures that convergence of the far canceller coefficients is achieved). The mean square error (MSE) is calculated for the error signal. Calculation of the MSE is obtained 200 symbol periods after the previously mentioned $1000T$ (T = one symbol period), i.e.

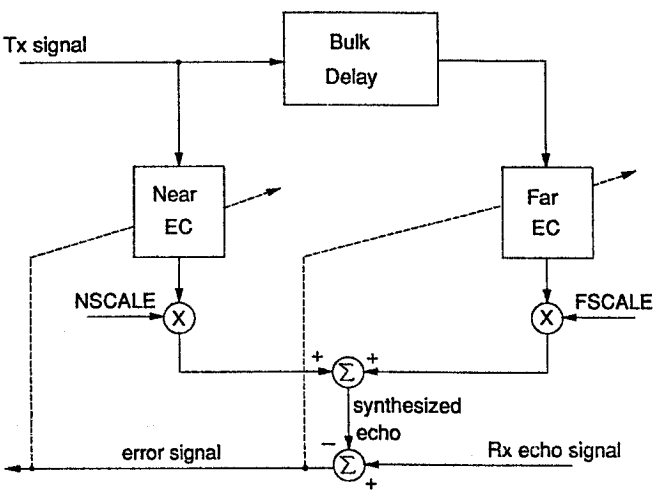

Figure 3. Scaling impulse responses.

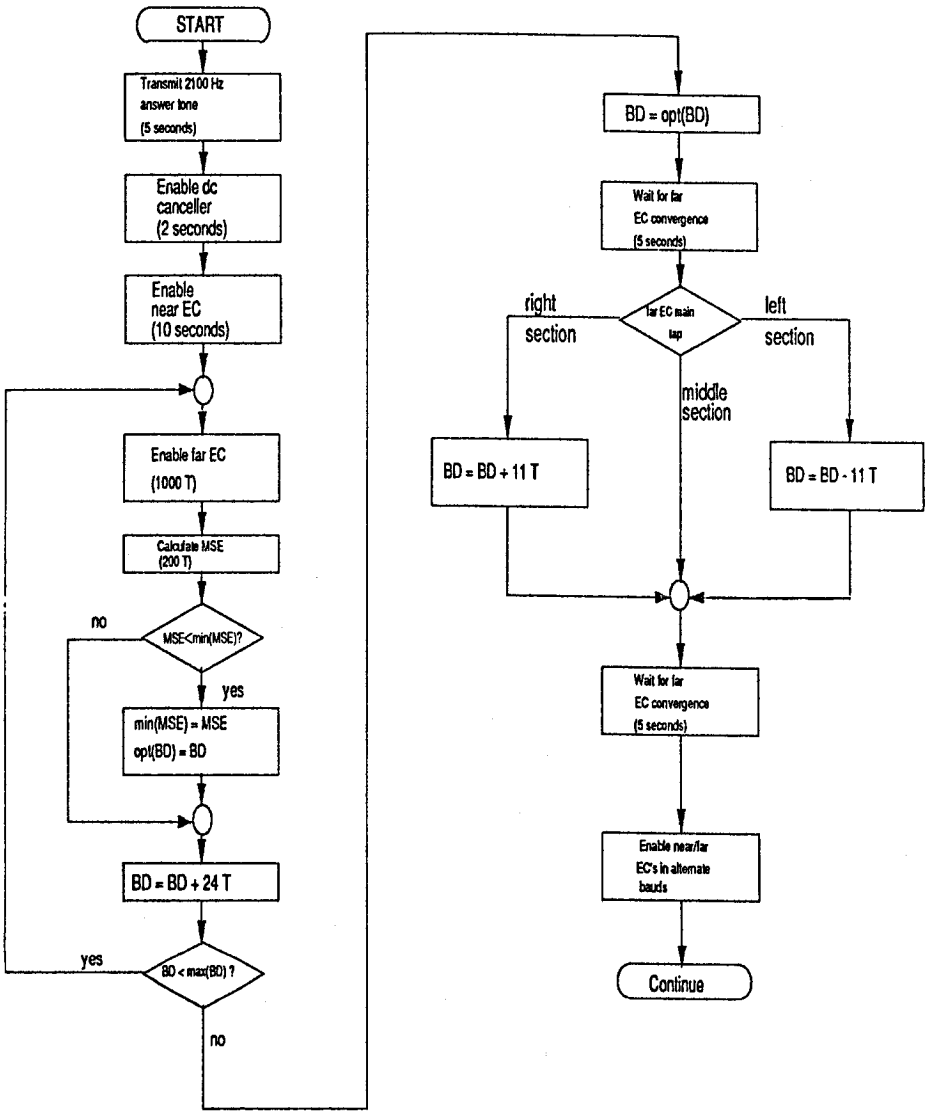

Figure 4. Flowchart for round-trip delay measurement.

after a total of $1200T$ corresponding to 500 ms. The bulk delay length is then increased by $24T$ (corresponding to 10 ms), and the process of updating and MSE calculation is repeated. With the far canceller delay line being $32T$, there will be $8T$ overlapping. This overlap is necessary to avoid having the far canceller main tap coefficient at the boundaries of the display. The MSE of the second step is compared with that of the first. The smaller MSE is kept, along with its bulk delay value. The process is then iterated by increasing BD by $24T$ each time, keeping track of the minimum MSE and its corresponding value of BD until its limit is reached. This upper limit is nearly $2400T$, corresponding to one second, which covers all satellite

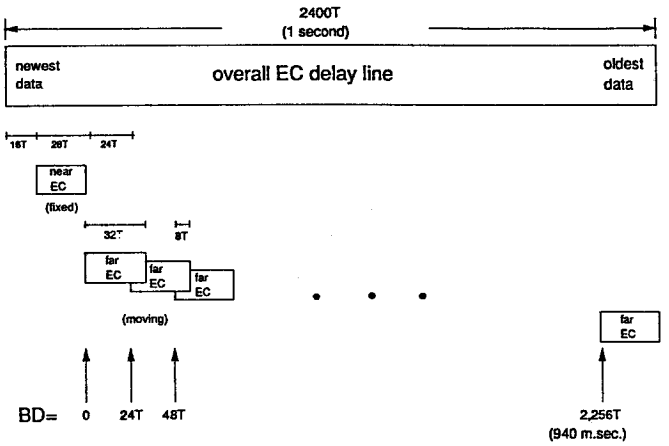

Figure 5. Moving window for round-trip measurement.

long round-trip delays (Tannenbaum 1981). Figure 5 shows a schematic diagram of this process.

For better resolution of the displayed far canceller impulse response on the PC screen, it is desirable to home the main (largest) tap coefficient to the middle section of the display. This is achieved in another program segment for fine measurement of the round-trip delay. The estimated round-trip delay is displayed (in milliseconds) on the screen along with the impulse responses of the near and far cancellers as well as the frequency offset (in hertz).

3.3. *The frequency offset*

To measure the frequency offset, a second-order phase locked loop (PLL) as shown in Fig. 6, is used. The phase comparator is obtained through the equation (Wang and Werner 1988):

$$\phi(t) \approx \mathrm{Im}\{e(t)\} \cdot \mathrm{Re}\{y_s^f(t)\} - \mathrm{Im}\{y_s^f(t)\} \cdot \mathrm{Re}\{e(t)\} \tag{2}$$

where Im and Re denote the imaginary and real parts, respectively, $e(t)$ is the complex error signal, while $y_s^f(t)$ is the complex synthesized far echo. Note that the

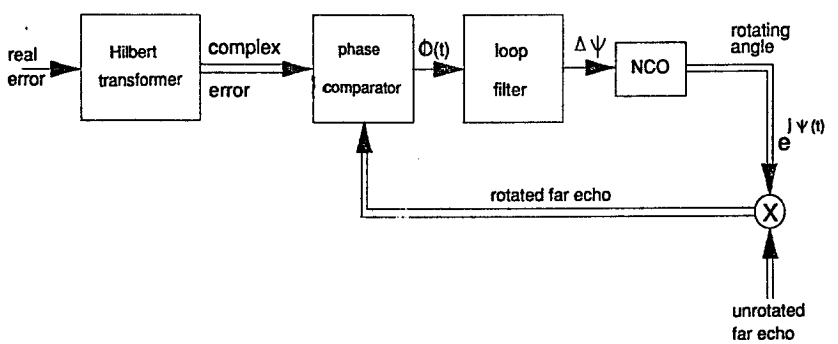

Figure 6. Phase-locked loop and accesories.

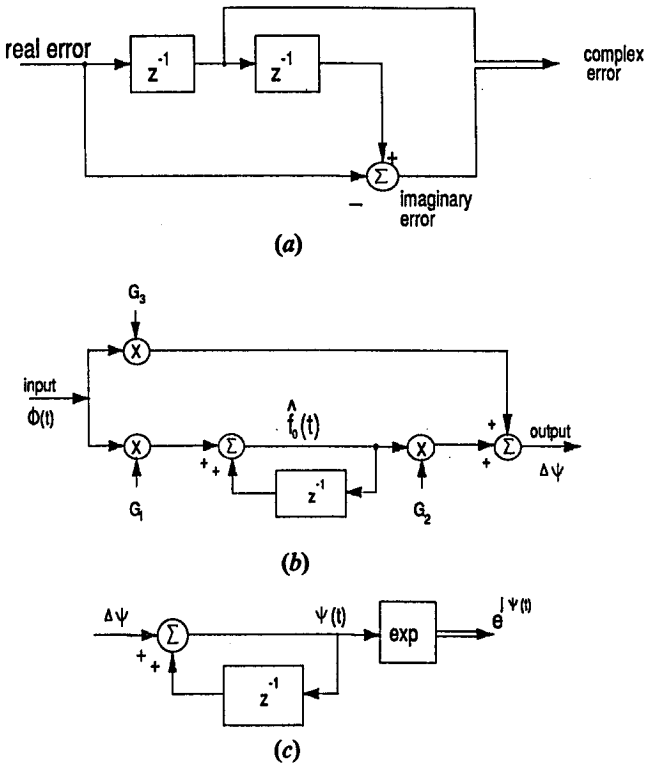

Figure 7. PLL components: (*a*) the Hilbert transformer; (*b*) the loop filter; (*c*) the NCO.

error signal is originally available as a real quantity representing the in-phase component. In order to obtain the imaginary part, which represents the quadrature component, a Hilbert transformer is used. To ease up the computational load, a simple two-tap Hilbert transformer is employed, as shown in Fig. 7(*a*), using the equation

$$\mathrm{Im}\{e(t)\} = \mathrm{Re}\{e(t-T)\} - \mathrm{Re}\{e(t+T)\} \tag{3}$$

The frequency offset measure $\hat{f}_0$ is achieved directly from a simple first-order loop filter according to the equation (see Fig. 7(*b*)):

$$\hat{f}_0(t) = \hat{f}_0(t-T) + G_1\phi(t) \tag{4}$$

where G_1 is a constant and $\phi(t)$ is the phase error obtained from (2). The phase roll increment $\Delta\psi(t)$ is also calculated using the loop filter through the equation

$$\Delta\psi(t) = G_2\hat{f}_0(t) + G_3\phi(t) \tag{5}$$

where G_2 and G_3 are constants. Finally, the numerically-controlled oscillator (NCO) is implemented with a simple accumulator according to (see Fig. 7(*c*)):

$$\psi(t) = \psi(t-T) + \Delta\psi(t) \tag{6}$$

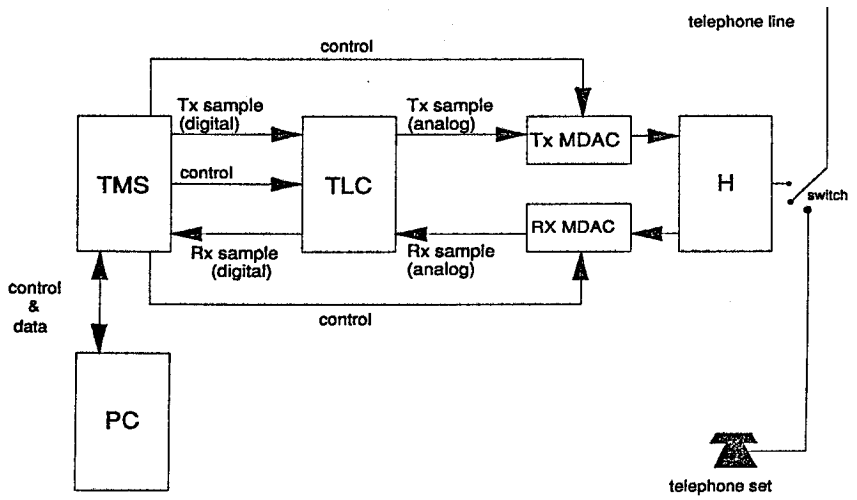

Figure 8. System hardware block diagram.

The choice of the loop filter constants (gains) G_1, G_2 and G_3 is crucial and depends heavily on experimentation and tuning. For example, if these gains are lower than necessary, convergence will be slow, and if they are higher than necessary, convergence will be erratic. If these constants are properly chosen, the PLL is said to be *well engineered* (Wang and Werner 1988). The system provides a compromise set of gain values, which is suitable for a wide range of channels. However, the user has the capability to change these gains according to the channel in hand. As a rule of thumb, high gains are needed for channels with high attenuation levels at the frequency band edges. For flat channels, however, low gains are needed.

4. Firmware of the proposed design

In this section, we present the hardware and software aspects of the proposed device. Initially, the overall picture of the system is given; then some details of each module of both aspects are considered.

4.1. *Hardware*

The hardware is depicted in the block diagram of Fig. 8. It consists of the following modules.

(i) The Compaq 386 Portable PC referred to as 'PC'.

(ii) The Atlanta (Chemira DSP board, which is based on the TMS320C25 DSP chip equipped with 128 kbyte RAM (Chemira 1988). This is referred to as 'TMS'.

(iii) The TLC32040 Analogue Interface (1987) chip which contains the A/D and D/A converters with 14-bit resolution for the received (Rx) and transmitted (Tx) samples, respectively. It is assumed that a single sampling rate of 7·2 kHz is used for both signals (synchronized). Accordingly, one interrupt routine is used. The chip is referred to as 'TLC'.

(iv) Adjustable gain control elements. The units are referred to as 'MDAC' (AD7546 1988). The control of the Rx and Tx levels should be given to the operator upon request.

(v) The hybrid, which performs the 2/4 wire conversion. It is referred to as 'H'.

4.2. *Software*

There are two main programming environments in the system. They are PC software and TMS software (see Fig. 9). Both execute and communicate with each other in real-time. In the following, we describe the functions of th routines.

4.2.1. *PC software.* The PC software is written in the 'C' language (Turbo-C), and it represents the host that the system operator deals with. The procedure is implemented as follows.

Step 1. Initially, a data entry menu is used to allow the user to enter data such as adaptation step size, transmit and receive scale factors, bulk delay limits, etc. The data entry menu is shown in Fig. 10.

Step 2. The PC puts the TMS processor on hold and transfers entered data to pre-defined RAM locations of the TMS.

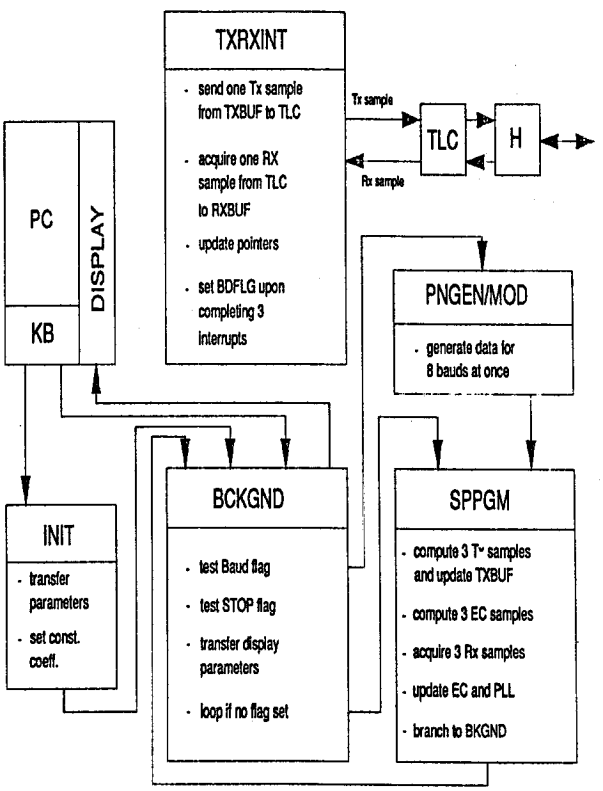

Figure 9. System software block diagram.

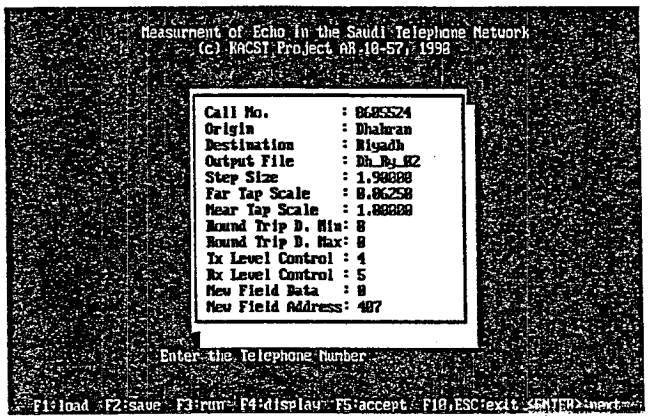

Figure 10. Data entry menu screen.

Step 3. The PC down loads TMS software into the TMS program RAM.

Step 4. The PC releases hold of the TMS, i.e. TMS software starts to run.

Step 5. Under the control of TMS, and using the polling method, the PC will acquire the results obtained through processing on the TMS, such as echo canceller (EC) taps, bulk delay (representing the round-trip delay), and the frquency offset. The process is repeated (partially) every baud (1 baud = 1 symbol = 3 samples).

Step 6. The PC displays the results, and draws the echo impulse responses on its monitor in real time in an iterative manner, i.e. the growth of the EC taps are observed. A display screen after processing is shown in Fig. 11. More details about Fig. 11 will be provided later in §4.

Step 7. At the end of the measurement, the PC saves all acquired and processed data in the output file and then returns to DOS.

The program allows the user to obtain a printout of the values of EC taps or a hard copy of the chart of EC taps representing the echo channel impulse response.

4.2.2. *TMS software.* For computational efficiency, the TMS software is written in the assembly language of the DSP chip (TMS320C25). The software consists of several modules, as follows.

Module 1. *Initialization module* (**INIT**), which performs the following.

(1) Programming the TLC where sampling rate, bandwidth of the anti-aliasing and reconstruction filters are provided. It also programmes the TLC to work in the synchronous mode.

(2) Defining and initializing the following.

(i) Vector for interrupt service routine (**TXRXINT**).

(ii) A sample counter (SCOUNT) and a baud flag (BDFLG). This flag is set by **TXRXINT** whenever three samples are received.

(iii) Baud counter (BDCOUNT). The use of this counter will be discussed later.

(iv) Transmit buffer (TXBUF) and receive buffer (RXBUF). Also **INIT** module defines and initializes 4 pointers. The first is the transmit buffer pointer (TXBPTR) used by the processing program to fill TXBUF. The second is the interrupt transmit buffer pointer (TXBIPTR) used by the interrupt service routine to send values from TXUBUF to TLC. The other two are the receive buffer pointer (RXBPTR) and the interrupt receive buffer pointer (RXBIPTR). Both buffers are circular to reduce processing time.

(v) RAM data for the transmit filter, echo canceller, etc.

Module 2. *Transmit receive interrupt routine* (**TXRXINT**).

The TLC32040 is an analogue interface chip especially designed to be used with the TMS320 family of DSP chips. The TLC can interrupt the TMS every time a transmit and/or a received sample is ready. In our case, one interrupt service routine is enough to take care of both the transmitted and received samples. **TXRXINT** sends and receives samles, and updates buffer pointers.

Module 3. *Processing programs.* This section is formed of two modules, as follows.

(1) Pseudo noise generator/modulator (**PNGEN/MOD**) module. This routine generates data for 8 bauds at one call. The word length of the TMS is 16 bits and hence it is more efficient to process 8 bauds at once. The 16-bit data are then encoded into QPSK where each two consecutive bits represent a baud. The data is then modulated. Owing to the convenient relationship between the baud (symbol) rate and the carrier frequency, modulation is achieved here by simply rotating the complex QPSK symbol with (0) quadrant for the first symbol, (1) quadrant for the second symbol, (2) quadrants for the third

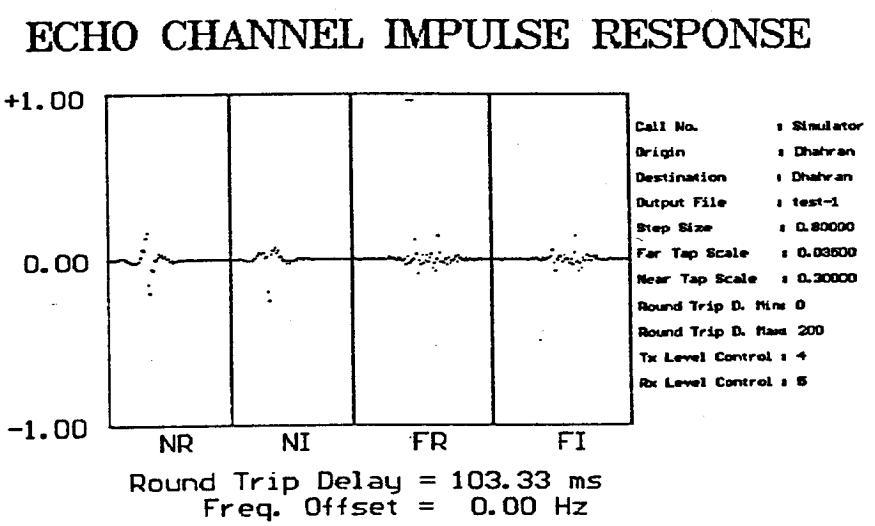

Figure 11. Display results of test-1 using a telephone channel simulator.

symbol, and finaly with (3) quadrants for the fourth symbol. The process is then repeated with the next (fifth) symbol treated as the first and so on. With the choice of generating 8 symbols at one call, the procedure becomes easy to implement. Note that all rotations are in the clockwise sense.

(2) Signal processing module (**SPPGM**): This is the main routine where processing of the transmitting and receiving data is taking place. It is executed once per baud. **SPPGM** performs the following.

(i) Computing 3 synthesized echo samples for one baud, with far echo samples obtained after rotation to compensate for the phase roll. This is achieved by convolving the modulator output with the current values of the EC taps. To make full use of the capability of the DSP chip (DMOV instruction), 300 words of the on-chip RAM are used for the delay lines. With each baud requiring two bits, this design can handle up to one second of round-trip delay. The near section of the canceller consists of 28 taps covering a time duration of 11·67 ms, while the far section contains 32 taps with 13·33 ms, i.e. the total time span is 25 ms.

(ii) Computing 3 Tx samples and placing them in TXBUF using TXBPTR. The transmit filter is based on interpolation, similar to the canceller. It consists of three sub-filters in the pass-band. The convenient relationship between the sampling and the symbol rates is again employed.

(iii) Acquiring 3 Rx samples.

(iv) Calculating the error between the actual received echo samples and the synthesized ones and using this error in updating the coefficients of the canceller and the PLL.

(v) Computing and compensating for the frequency offset. This is basically achieved as explained earlier. The 3 (real) error samples are used to generate one complex sample. This complex sample consists of the second input sample as the real part and the Hilbert transform sample as the imaginary part, using (3) and as shown in Fig. 7(*a*). The rotating angle $\psi(t)$ is obtained as depicted in Fig. 7, using (2)–(6). The delay lines of the far canceller are then updated by the rotating angle $\psi(t)$, once per baud. The frequency offset is measured by the program location **FREQ**, which represents f_0 in our analysis.

(vi) Returning to 'background routine', which is explained next.

At the start-up of testing, the SPPGM module uses a timer for the following operations (see Fig. 4).

(*a*) Transmitting a tone of 2100 Hz for 5 s with phase reversal every 450 ms to disable network echo suppressors.

(*b*) Nullifying the DC bias that might take place in the receive signal due to the A/D converter which employs a simple one-tap canceller that adaptively cancels any DC drift.

(*c*) Estimating the bulk delay by placing the far canceller sequentially in adjacent locations across the 300-word delay line and selecting the optimum position, which produces the minimum mean squared error. This process may take a long time (up to one minute) because, for

each position, the far canceller has to converge. The duration can be reduced by setting a maximum bulk delay in the data entry menu.

Rotating the complex far echo signal and obtaining the answer tone of 2100 Hz are achieved through a 2k-word sine look-up table.

Module 4. *Background module* (**BCKGND**). This module communicates and passes parameters to all other modules as follows.

(1) It uses the time slot between the consequent received bauds to communicate with the PC programmes and transfers processing results (EC taps, bulk delay, etc.). The results are then displayed on the PC screen continuously in real-time by the PC program.

(2) Resets BDFLG and branches to processing programmes according to the state of BDCOUNT. This is mechanized as follows.

(*a*) When BDCOUNT is zero, it branches to the **PNGEN/MOD** module, which generates a new set of 8 bauds. Then it proceeds to **SPPGM**.

(*b*) If BDCOUNT is not zero, it branches directly from the background routine to **SPPGM**.

5. Laboratory and field testing

In order to evaluate the proposed system, quantities, that are known *a priori* are measured and compared with the real ones. Testing and tuning of the developed software are achieved mainly through the use of the telephone channel simulator (Model PTT 5100/5151, manufactured by Processing Telecom Technologies Inc.) by presetting certian parameters and then allowing the system to measure them. Here, we present the results of performing three tests, test-1, test-2 and test-3. In test-1, a flat channel is introduced in the forward path with an attenuation of 20 dB. The reverse attenuation is set to 12 dB. A far echo is inserted, with a delay of 100 ms and an attenuation of 15 dB. No freuqency offset is present in the far echo. The result of test-1 is shown in Fig. 11, which is a print of the PC display. The parameters entered in the data entry menu are also displayed for convenience. The leftmost two sections of the displayed graph are for the near echo channel (real and imaginary indicated by NR and NI, respectively), while the other two sections are for the far echo channel. The measured round-trip delay is, as shown, 103·33 ms. The difference of 3·33 ms is primarily due to the positioning of the largest tap coefficient in the middle section of the far echo model (see Fig. 4). The frequency offset is properly measured with zero frequency.

In test-2, the simulator is arranged with the same settings as test-1 except that the flat channel is replaced with the M.1025 model of the CCITT. Results are shown in the display of Fig. 12. Note that the far echo is dispersed further, while the near is unchanged. The far scale factor (FSCALE) has to be decreased from 0·03 to 0·025 (in comparison with test-1) in order to enlarge the displayed far echo. The round-trip delay and the frequency offset are properly measured.

In order to test the system capability of measuring the frequency offset, the simulator is kept with the settings of test-2 with the exception of introducing a frequency offset of 1 Hz. This last test is called test-3, where the results are displayed in Fig. 13, showing the proper measurement.

The developed system has been used in the field by testing echo in the Saudi telephone network, both at the national and the international levels. Figure 14

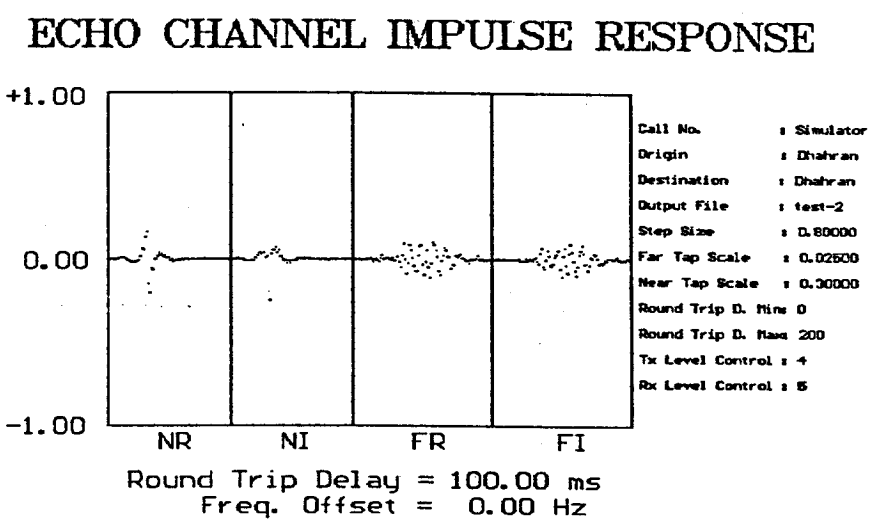

Figure 12. Display results of test-2 using a telephone channel simulator.

shows the results of a real telephone connection between the City of Al-Ain in the United Arab Emirates (UAE) and the City of Dhahran in Saudi Arabia. The test was made in Al-Ain. The round-trip delay is measured as 523·33 ms. Since the distance between the two cities is less than 1000 km, it is evident that this call must have included a satellite link. This is another dimension added to the features of the proposed device, that is, distinguishing between satellite and terrestrial calls. The results of Fig. 14 also indicate a measured frequency offset of −0·11 Hz. In addition,

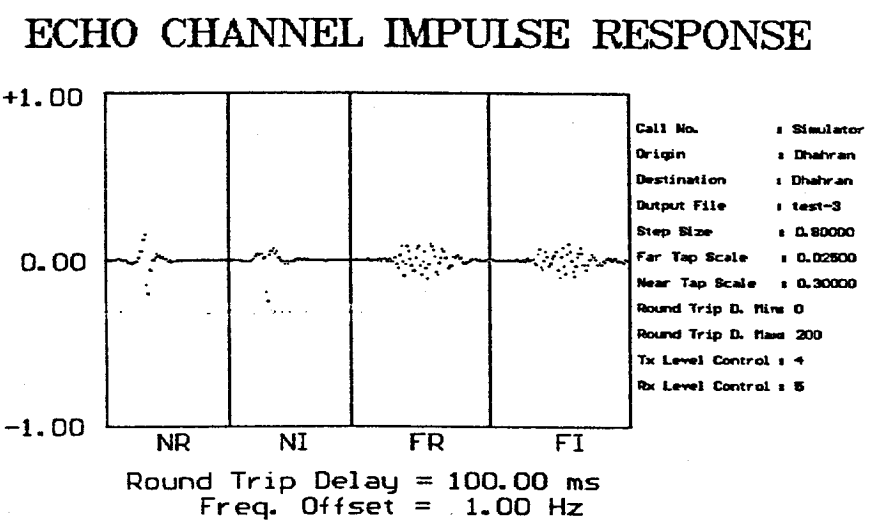

Figure 13. Display results of test-3 using a telephone channel simulator.

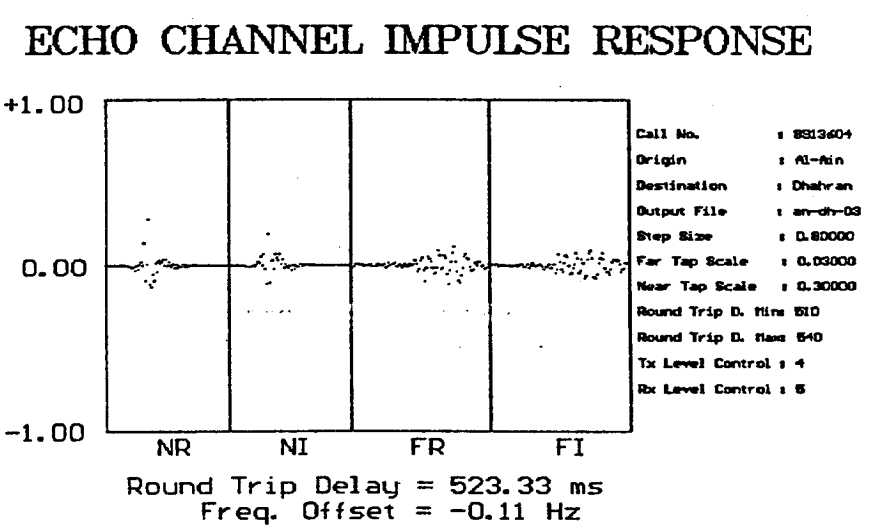

Figure 14. Display results of a real telephone connection—source: Al-Ain, UAE; destination: Dhahran, Saudi Arabia.

comparing the impulse responses of both near and far echoes of this test with those of other tests performed using the simulator, we find that the near echo impulse response is totally different. This is expected because the subscriber loop is different. On the other hand, we can see that the far echo of the field test resembles an M.1025 channel.

6. Conclusion

A schematic design for a versatile test device to measure all aspects of echo in GSTN is proposed. Echo parameters are reviewed and identified first, and a measurement strategy based on echo cancellation is presented.

The proposed design is based on a general-purpose microcomputer and an off-the-shelf digital signal processing board with minimum additional hardware. This makes the proposed device fully programmable and compatible with existing design components.

The hardware and software components of the proposed design are presented. Although specific hardware is used in implementing the proposed device, any similar structure based on different components can be used with the same strategy.

The proposed system is tested under laboratory conditions using a telephone channel similator, as well as in the field. Results of these tests are included.

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