

School of Computer Science

Ph.D. Final Defense

by

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Reconfigurable Microprocessors: Instruction Set Selection, Code Optimization, and Configuration Control

In contrast to a conventional microprocessor, the architecture of the hardware and/or the instructions supported by a reconfigurable microprocessor can be changed dynamically. This means that the type and quantity of circuitry implementing certain instructions, or other functionality, can be changed after fabrication of the processor and, in some cases, even during execution. This ability to configure a processor to implement functionality targeted towards a specific application or application domain provides an opportunity to improve the performance of the application, the processor, and the supporting system(s) in terms of speed, power, size, and weight.

Several approaches to the design and implementation of reconfigurable processors are explored and analyzed with the goals of making the design and use of reconfigurable processors more attractive and accessible. The two areas targeted are the design and use of (1) customized processors that are typically utilized in embedded systems and (2) general-purpose superscalar processors. A new approach for the customization of application specific processors by selecting instructions to be supported by the processor using reconfigurable hardware is presented. Next, this type of processor is expanded to allow the custom extensions to be altered dynamically while an application is being executed. A major concern in such a processor is the overhead required to alter the hardware of the processor. An instruction re-ordering approach is proposed and studied with the goal of mitigating this overhead.

The second area of work presented is the design and implementation of a general-purpose superscalar processor with the goal of improving the instruction level parallelism (ILP) achieved by the processor architecture. The ILP is increased by introducing execution units into the architecture that can be dynamically altered to support the instructions that are currently being executed by the processor. The contribution of this work is an efficient micro-architectural solution to the management of the various configurations of the execution units that can be dynamically loaded into the architecture. This management approach effectively steers the current configuration of the execution units toward a configuration that is well matched with the requirements of the instructions being scheduled for execution.

Date: Friday, December 2, 2005

Time: 2:00 P.M.

Place: Computer Science Conference Room, EL 139

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